



Altera® Application Solutions Guide Book

December 2011

Prepared by



MACNICA Group Companies

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Introduction to Macnica Group

Altima Corp., Elseno, Inc., Cytech Technology Ltd. and Galaxy Far East Corp. are the Macnica Group companies with the common supplier - Altera Corporation - in their line card and the common corporate culture aiming at providing the customers with high level of technical solutions in addition to selling the products.

About Macnica Group



Macnica Group is one of the largest full-service electronics and networking systems distribution companies in the world with the headquarters in Yokohama, Japan. Macnica provides the most advanced and high added-value electronics products including semiconductor devices, electronics components, network related equipment, software products to various electronics OEMs and customers in the world.



Since its foundation in 1972, Macnica has focused in technical support and deepened its technical strengths,

leading the industry in establishing the technical-support centric business style. **“The Engineering Distributor”** is the new category of distribution models in the electronics industry built based on the style of Macnica Group.

The distinguished technical and engineering strengths... The ability to find new prospering product lines that grew in the wide range of

business relationship with the numerous startups born every day throughout the world... The value proposition presented to customers by truly understanding their technical issues and leading to the best solutions... Those are all the strengths with Macnica. All the employees are sharpening these strengths so that the value they bring to the customer becomes optimal.

Macnica also has focused in expanding its global network by establishing subsidiaries in the US, Europe and in Asia Pacific area. With the offices in 34 locations worldwide, Macnica Group looks into becoming the best of the kind in the world in the Engineering Distribution model.

Now Macnica is climbing to its new height by disrupting the Engineering Distributor model by itself. Becoming more like what we are... Seeking the things only Macnica can attain... With those questions in mind Macnica has reached to the stage to bloom to become **“The Demand Creation Distributor”** who identifies the potential demand within the customers and in the market by utilizing its business foresight

and technical insight. Macnica will find things existed nowhere and bring them here for you. Macnica Group keeps going, with challenges. “NOWHERE, but **HERE.**”

Macnica Group Facts

Established	October 30, 1972	
President & CEO	Kiyoshi Nakashima	
Paid-in Capital	JPY 11,194,268,000 (as of March 31, 2011)	
	Publicly traded at The 1 st Division of Tokyo Stock Exchange (Symbol: 7631.t)	
Revenue	FY06	JPY 163.6 Billion
	FY07	JPY 154.1 Billion
	FY08	JPY 131.5 Billion
	FY09	JPY 149.2 Billion
	FY10	JPY 188.4 Billion
Employees	1,555 (Group World Wide Total: as of March 31, 2011)	

Group Structure and Subsidiaries

Macnica Group consists of Macnica, Inc. with three internal division companies covering Japan, five subsidiaries covering Japan, Macnica brand subsidiaries in the USA, Europe and Asia, and subsidiaries covering Asia Pacific, ASEAN countries and India.

JAPAN

-  Macnica, Inc.
 - Corporate Headquarters
 - Division Companies
 -  Clavis Company
 -  Brilliant Technology Company
 -  TecStar Company
-  **Altima Corp.** 
-  **Elsena, Inc.** 
-  Kogent, Inc.
-  Macnica Networks Corp.
-  Macnica Solutions Corp.

HONG KONG / CHINA

-  Macnica Hong Kong, Limited.
-  Macnica Shanghai, Limited.
-  **Cytech Technology Ltd.** 

TAIWAN

-  Macnica Taiwan, Limited.
-  **Galaxy Far East Corporation** 

KOREA

-  Macnica Korea, Limited.

SINGAPORE / ASEAN

-  Macnica Asia Pacific Pte Ltd.
-  Macnica (Thailand) Co. Ltd.
-  **Cytech Global Pte. Ltd.** 

INDIA

-  **Cytech Global Pte. Ltd.**

USA

-  Macnica USA, Inc.
-  Macnica Networks USA, Inc.
-  **Macnica Americas, Inc.** 

EUROPE

-  Macnica GmbH

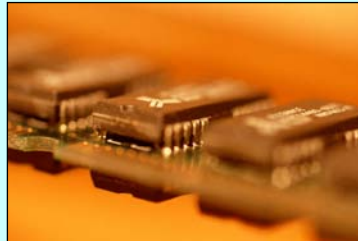
Altera® Application Solutions Guide Book – November 2011

Altima Corp., Elseno, Inc., Cytech Technology Ltd. and Galaxy Far East Corp. are the Macnica Group companies with the common supplier Altera Corporation in their line card and the common corporate culture aiming at providing the customers with high level of technical solutions in addition to selling the products.

This guide book “Altera® Applications Solutions Guide Book,” co-edited by Altima, Elseno, Cytech and Galaxy, provides the information beneficial for the customers who are trying to solve their problems in FPGA designs in specific applications such as video processing, high speed memory interface, high speed serial interface, embedded system designs and ASIC prototyping.



1. Video Processing



2. High Speed Memory Interface



3. High Speed Serial Interface



4. Embedded System Design



5. ASIC Prototyping

Video System Solutions

Your Video System Design Starts Here ...

Before you start your next video system design, check out the largest, most comprehensive collection of video solutions in the FPGA industry.

By building your next design using Altera® video intellectual property (IP), reference designs and development kits, you'll be able to take full advantage of Altera's innovative FPGA features, including:

- Inherently parallel digital signal processing (DSP) blocks
 - An abundance of embedded memory blocks
 - A large number of registers
 - High-speed DDR memory interfaces
-

Altera video system solutions have three components to help you create the most dependable system design and finish development fast:

1. **Altera Video Design Framework** – This is a combination of IP cores, interface standards and system level design tools that are developed to enable a plug-and-play video system design flow. Altera provides a comprehensive suite of video function IP blocks that can be connected together to design and build video systems. Plus, designs built using the Altera video design framework are open, allowing you to easily replace an Altera IP with your own custom function block.
2. **Suite of Video reference designs** – Reference designs created by Altera as well as our partners and built using the Altera video design framework. This substantial suite of image format conversion reference designs are hardware verified and available immediately to serve as the starting point for your application.
3. **Range of DSP Dev Kits for Video** – Kits, also designed by Altera and our partners, to help you prototype your video system design. These kits support a range of video I/O formats (such as SDI, ASI, DVI, HDMI, Composite and VGA), and are based on our highly regarded Stratix®, Arria® and Cyclone® FPGA families.

1080p Video Design Framework

Altera developed a video design framework that enables the fastest design cycle for video application. The components of this framework are:

- A library of basic building block video image processing intellectual property (IP) cores designed for easy plug-and-play type interface
- A low-overhead streaming video interface protocol, which is available as an open standard
- System tools such as SOPC Builder that allow for an automated way of generating control and arbitration logic
- A suite of HD reference designs that can be used as a starting point for your video datapath designs

Figure 1 shows the suite of IP cores that are part of a video image processing suite of IP cores. This suite provides IP that ranges in complexity from a color space converter to a polyphase scaler and motion adaptive de-interlacer.

The Avalon® Streaming interface (ST) video protocol is designed for sending dvideo and control data from one video processing block to the other.

This protocol is open and the specification is freely downloadable via the web. Using this specification does not in any way lock you to Altera® FPGAs, but all the Altera video IP and video reference designs utilize this interface.

Figure 2 shows how different video functions can be connected using this protocol. More information on this protocol is available in the 'Interface' section of the Video and Image Processing Suite User Guide (PDF).

Video systems almost always include an embedded processor and a memory subsystem to manage the video frames in the external memory. The SOPC Builder system tool provided by Altera greatly simplifies embedded system design. This tool includes a library of elements such as soft core processors (Nios® II), interfaces, memory, bridge, and DSP IP cores. It also features a connectivity GUI and generator

to automatically wire up arbitrated and streaming bus systems.

Figure 1 Complete Suite of Video Image Processing IP

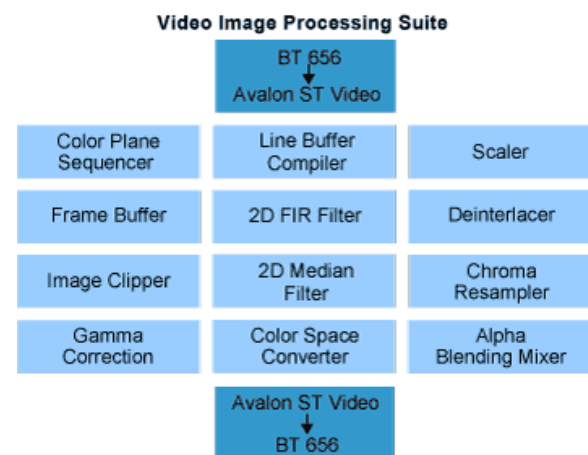
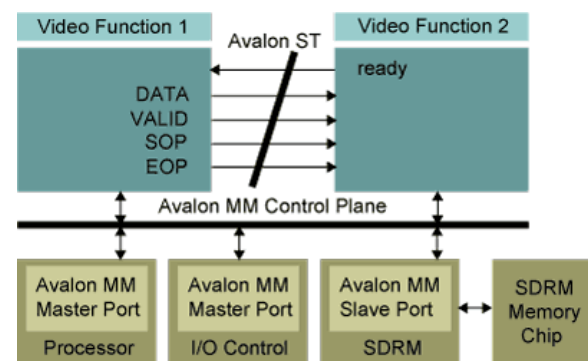


Figure 2 Avalon ST Protocol for Video Interfaces and Avalon Memory Mapped (MM) Protocol for Control Plane Interfaces



Finally, the entire video design framework really comes together in the form of an HD reference design that showcases the actual video processing common to many applications. Altera developed several reference designs that were driven by actual customer demand for scaling, mixing, and processing HD video streams over serial digital interfaces (SDI).

Figure 4 shows one of the reference designs that processes 1080p quality video. This design was built using the Altera video design framework. For more details on this design contact your local Altera FAE.

Figure 3 SOPC-Based Design Flow for Video Datapaths

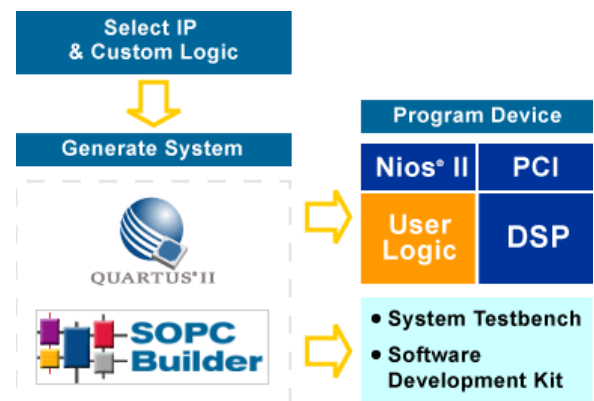
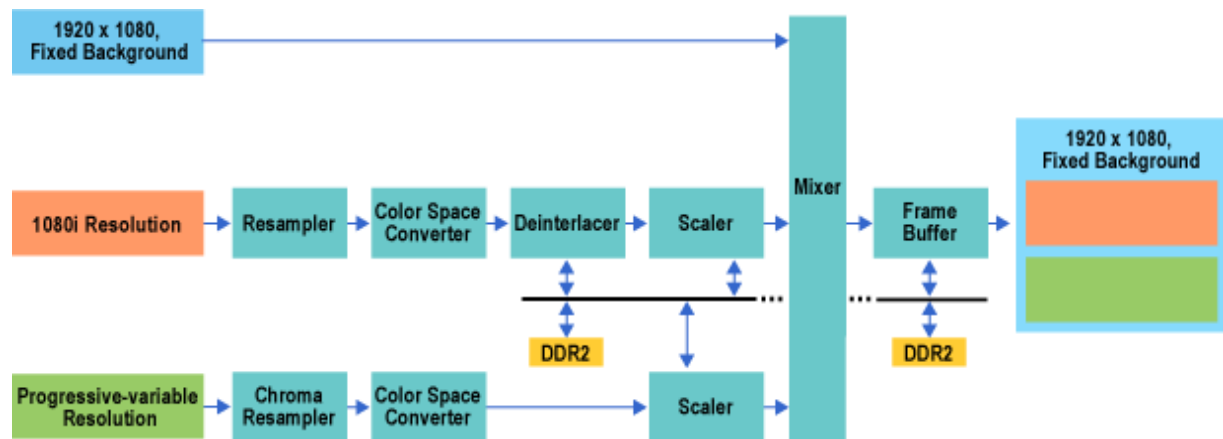


Figure 4 HD Quality Reference Designs to Speed Development



Video Reference Designs

Altera provides one of the largest portfolios of video processing designs – all built using the Altera VIP suite of video cores.

1. The Altera video and image processing example design demonstrates dynamic scaling and clipping of a standard definition video stream in either NTSC or PAL format and picture-in-picture mixing with a

background layer. The video stream is output in high definition resolution (1024×768) over a digital video interface (DVI). This design is fully verified on the Cyclone III Video development kit.

Core	Description
Deinterlacer	Converts interlaced video formats to progressive video format
Color Space Converter	Converts image data between a variety of different color spaces
Scaler	Resizes and clips image frames
Alpha Blending Mixer	Mixes and blends multiple image streams
Gamma Corrector	Performs gamma correction on a color space
Chroma Resampler	Changes the sampling rate of the chroma data for image frames
2D Filter	Implements 3x3, 5x5, or 7x7 finite impulse response (FIR) filter on an image data stream to smooth or sharpen images
2D Median Filter	3x3, 5x5, or 7x7 filter that removes noise in an image by replacing each pixel value with the median of neighboring pixel values
Line Buffer Compiler	Efficiently maps image line buffers to Altera® on-chip memory

2. Various format conversion reference designs that use the SDI video input – primarily used in broadcast applications. These designs feature two-channel up/down/cross conversion that entails polyphase scaling,

motion adaptive deinterlacing, mixing and frame rate conversion for resolutions up to 1080p. These designs have been verified on the Stratix II GX Audio Video development kit.

Reference Design	Demo Board	Features
UDX 3.1 Reference Design	Stratix® IV GX FPGA Development Kit	- Multi-channel format conversion with selectable inputs and outputs - Features multi-port front-end memory controller (with efficiency > 90%) - Supports DVI, HDMI, SDI interfaces - Run-time configurability - Active Format Descriptor (AFD) extraction and insertion *Contact Altera Sales for design
Format Conversion Reference Designs (v1)	- Stratix II GX Audio/Video Development Kit - Stratix IV GX FPGA Development Kit	- Two-channel up/down/cross conversion: polyphase scaling motion adaptive deinterlacing, mixing and frame rate conversion for resolutions up to 1080p - SDI, DVI, DDR2 memory interfaces - Run-time configurability of functions using the Nios® II embedded processor - Output run-time configurable to 480p/720p/1080p
Format Conversion Reference Designs (v2)	- Stratix II GX Audio/Video Development Kit - Stratix IV GX FPGA Development Kit - Arria II GX FPGA Development Kit	- Two-channel up/down/cross conversion: polyphase scaling motion adaptive deinterlacing, mixing and frame rate conversion for resolutions up to 1080p - SDI in/SDI out, DDR2 memory interfaces - Run-time configurability of functions using the Nios II embedded processor - Outputs both interlaced and progressive
NTSC-to-HD Scaling	Cyclone® III Video Processing Development Kit	- Up conversion of NTSC video to 720p using polyphase multi-tap scaling and motion adaptive deinterlacing - Picture-in-picture (PIP) mixing with test pattern background - Composite in/DVI out - Color space conversion, chroma resampling, frame buffering, alpha blending, and memory controller

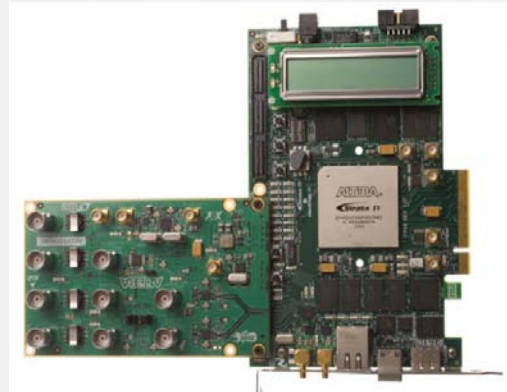
3. Altera's partner Bitec has developed multiple reference designs that work with Cyclone III Video Dev Kit. Visit Altera web site to get designs that showcase color space conversion, Picture-in-Picture, 4-channel video compositing and even a 1080p H.264 encoder design.
4. Altera's partner Microtronix has also developed a portfolio of video reference designs that are available with their Stratix III Broadcast IP Dev Kit and with their Cyclone III ViClaro Video Dev Kit.

These designs use the Altera VIP functions in conjunction with high bandwidth memory efficient, Microtronix Avalon Multi-port DDR2 Memory Controller for building high-resolution video broadcast systems. The designs showcase motion-adaptive deinterlacing, dynamic scaling and graphics overlay.

These reference designs are available with the purchase of the development kits from Microtronix.

Video Development Board Solutions

Audio Video Development Kit, Stratix IV GX Edition



ALTERA Altera Corporation

The Audio Video Development Kit, Stratix IV GX Edition, delivers a complete video and image processing development environment for design engineers. The kit facilitates the entire design process, from design conception through hardware implementation.

Features

- Altera Stratix IV EP4SGX230KF40C2N
- The kit is the combination of:
 - **Stratix IV GX FPGA Development Board**
 - The transceiver serial digital interface (SDI) high-speed mezzanine card (HSMC)
- Video/audio interfaces

- HDMI video output on the FPGA host board
 - One 3G-SDI video input and output on the FPGA host board
 - Two additional SDI inputs and outputs for triple-rate SDI supporting 3G, and high-definition (HD) and standard-definition (SD) standards on the HSMC
 - Two AES inputs and outputs on the HSMC
 - Memory devices
 - 512-MByte DDR3 SDRAM with a 64-bit data bus
 - 128-MByte DDR3 SDRAM with a 16-bit data bus
 - Two 4-MByte QDR II + SRAMs with 18-bit data buses
 - 64-MByte sync flash and 2-MByte SSRAM external memory
 - Loopback and debug HSMCs
 - Design examples: Board Update Portal and Board Test System
 - OpenCore Plus access to the MegaCore® IP library, including the Altera Video and Image Processing Suite of intellectual property (IP) cores
- SDI reference design

Arria II GX FPGA Development Kit



ALTERA Altera Corporation

The Altera Arria II GX FPGA Development Kit delivers a complete system-level design environment that includes both the hardware and software needed to immediately begin developing FPGA designs. With this PCI-SIG-compliant board and a one-year license for Quartus II design software, you can:

- Develop and test PCI Express 1.0 (up to x8 lane) designs
- Develop and test memory subsystems consisting of DDR2 and/or DDR3 memory
- Develop and test designs based on other Arria II GX supported protocol interfaces such as Gigabit Ethernet, SDI, CPRI, OBSAI, SAS/SATA, and Serial RapidIO.

Features

- Altera Arria II GX EP2AGX125EF35 FPGA
- On-board ports
 - One HSMC expansion port
 - One gigabit Ethernet port
- On-board memory
 - 128-MB 16-bit DDR3 device
 - 1-GB 64-bit DDR2 SODIMM
 - 2-MB SSRAM
 - 64-MB flash
- On-board clocking circuitry
 - Four on-board oscillators
 - ✧ 100 MHz
 - ✧ Programmable oscillator, default frequency 125 MHz
 - ✧ Programmable oscillator, default frequency 100 MHz
 - ✧ 155.52 MHz
- General user I/O
 - SMA connectors for clock input/output
 - LEDs/displays

Cyclone III FPGA Development Kit

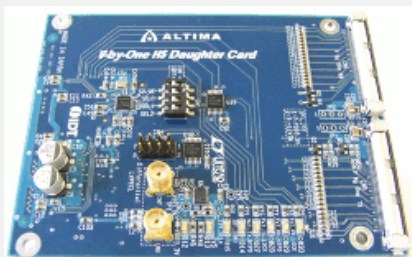


Altera Corporation

Altera's Cyclone III FPGA Development Kit combines the largest density low-cost, low-power FPGA available with a robust set of memories and user interfaces. The kit dramatically reduces the design and verification portion of your project, whether it's for automotive, consumer, wireless communications, video processing, or another high-volume, cost-sensitive application.

Features

- Cyclone III development board
 - Cyclone III EP3C120F780 FPGA
- Embedded USB-Blaster™ circuitry (includes an Altera MAX II CPLD) allowing download of FPGA configuration files via the flash device or the host computer
- Memory
 - Dual-channel DDR2 SDRAM (w/ECC 256MB)
 - SSRAM (8MB), Flash (64MB)
- Communication ports
 - 10/100/1000 Ethernet
 - USB 2.0
- Clocking
 - SMA inputs/outputs
- Display
 - 128 x 64 graphics LCD
 - 2-line x 16-character LCD
- Connectors
 - Two HSMCs
 - USB type B
- Debug tools
- Cyclone III FPGA Development Kit CD-ROM (download all CD contents via FTP)



V by One HS x8 Daughter Card



ALTIMA ALTIMA Corp.

The daughter card to evaluate THine V-by-One®HS x8 signals. This card is used with a development kit with HSMC connector.

Features

- Supports up to 8 pairs of V-by-One HS streams
- Supports V-by-One HS IP core developed by Macnica with license from THine Electronics, Inc.
- FX16 connectors compliant to V-by-One HS standard
- Interfaces:
 - HSMC
 - V-by-One
 - I2C for clock frequency configuration
- Linear Technology LT3029
- IDT 5V49EE504
- HIROSE FX16 Right Angle x51
- Silicon Lab Si5317
- Samtec QTH-090-01-L-D-A



SDI Daughter Card



ALTIMA ALTIMA Corp.

The daughter card to evaluate SDI signals. This card is used with a development kit with HSMC connector.

Features

- Supports up to 8 pairs of SDI streams
- Supports Altera MegaCore SDI IP core
- Designed by using active SDI connectors with built-in cable drivers and equalizers to attain small board size and higher signal integrity
- Interfaces:
 - SDI x 8 channels
 - SMA (External CLK input)
 - SMA (CLK output for evaluation)
- Linear Technology LT3029
- IDT 5V49EE504, ICS810001-22, ICS8535-21
- Canare BCA-TL/LF
- Samtec QTH-090-01-L-D-A

Board Solutions from Third Party Board Partners



FE-4CGX150



Hangzhou Free Electron Co. Ltd

Altera Cyclone IV GX FPGA development platform

Features

- FPGA : EP4CGX150DF27C8
- Config: support FPP, support 4 different config
- Sync SSRAM: CY7C1360C-200AXC
- DDR2 SD RAM: 32bit, 128M Byte
- SFP: 1 channel, support as fast as 3.125G
- Gigabit Ethernet port: 1 Channel, Marvell 88E1111-CAA1
- USB2.0 : slave mode/ FIFO, FT232HL
- PLL circuit : 5M-500MHz
- 1 x high precision active X'tal
- PCI-E: PCI-E 1.1 X 4
- 1 x 8 DIP switch
- 4 LED O/P
- HSMC expandable slot
- Power supply to support 12A to Core chip, 5A configurable VCCIO

Daughter Cards

USB 2.0 + Gigabit Ethernet



SD/HD-SDI



2 CH high speed AD/DA 105M



Dual 100M Industrial Ethernet



Audio / Video



Features

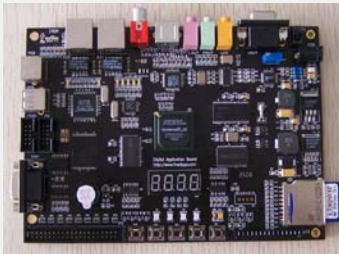
- Audio AD/DA, 1 x I/P, 2 x O/P
- 24bit true color VGA port
- Video decoding : support ITU-R BT.656 YCrCb 4:2:2(16bit/8bit), 1 CH S_VIDEO

HSMA SMA IO expandable



Features

- 60 x I/O
- 1 x 8bit DIP switch
- High speed transceiver :RX, TX
- Input clock: CLKIN x1; Output clock: CLKOUT x 2
- 4 LEDs
- 4 SMA signals



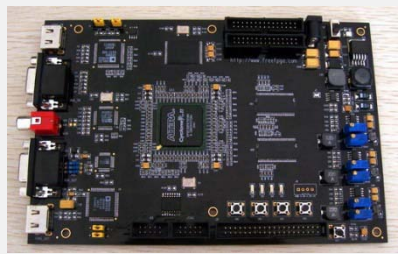
Digital Application Dev Board



Hangzhou Free Electron Co. Ltd

Features

- ALTERA Cyclone II EP2C35F484C8
- Offer uClinux OS including network support (DHCP, tftp, web)
- 64M Byte SDRAM
- 32M Byte FLASH
- 2 independent 512K bit SRAM
- Two 100M Ethernet interface, one use 100M PHY, can verify Altera tri-speed Ethernet IP, the other use 100M Ethernet MAC/PHY
- Support ITU-R BT.656 YCrCb 4:2:2 (16bit/8bit) video output, 1 CVBS, 1 S-Video interface
- Support SD card
- USB1.1 interface, 24 bit VGA, PS/2



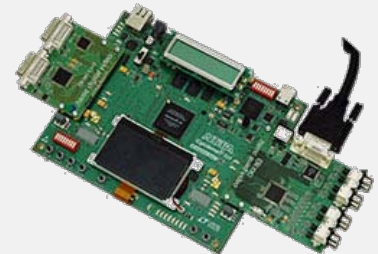
Video Dev Board



Hangzhou Free Electron Co. Ltd

Features

- FPGA: ALTERA Cyclone II EP2C35F672C8
- 8 layer PCB
- 64M Byte DDR SDRAM
- 32M Byte FLASH
- can plug 100M ETHERNET PHY daughter card
- 1x CVBS, support ITU-R BT.656 YCrCb 4:2:2 (16bit / 8bit)
- LVDS in/out, support video transport
- 1 x 24bit VGA input and output
- 1 x HDMI input/output
- 40 x expand IO (2 x CLK, 2 x PLL1output, 36 x IO)



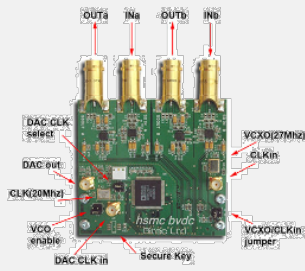
Cyclone III Video Development Kit



Bitec Ltd.

Features

- Altera EP3C120F780 Development board
- Bitec HSMC Quad Video daughter card
- 8 composite or 4 s-video inputs
- 1 HD (1080p) DVI Output port or
- 1 TV (PAL/NTSC) output with resolutions to 1024x768 and support for composite, s-video or SCART (RGB) outputs
- Bitec HSMC DVI daughter card
- 1 HD (1080p) DVI Output port (HDMI with external adaptor)
- 1 HD (1080p) DVI Input port (HDMI with external adaptor)
- Interfaces directly to the Altera Video and Image Processing (VIP) Suit
- Collection of video reference designs



Broadcast Video Card

Bitec Bitec Ltd.

Develop professional video fpga based systems using the Bitec BVDC.

Features

- Dual ASI/SD-SDI transmitter/receiver
- Adaptive cable equalizers
- Multi-rate cable drivers
- 27 Mhz VCXO
- 200Mhz Quadrature Modulating 14-bit DAC



DVI Input/Output Card

Bitec Bitec Ltd.

Two channel Dual-Link DVI output board for Altera FPGA development kits with HSMC expansion port.

Features

- Single link operation from 25-165 Megapixels per second (VGA to UXGA)
 - Dual link operation up to 330 Megapixels per second (3200x2400)
 - EDID reading/writing
 - 12-bit (½ pixel) DDR input with flexible input clocking: Single-clock/dual-edge or dual-clock/single-edge
 - I2C slave programming interface
 - Cable distance support: Over 10 m
 - Monitor detection through Hot-Plug
- Compliant with DVI 1.0



Cyclone III SDALTEVK Kit

Bitec Bitec Ltd.

Features

- Altera EP3C120F780 Development board
 - National Semiconductor's HSMC SDI video and clocking daughter card (SDALTEVK)
 - Supports SD, HD and 3G-SDI (SMPTE 259M-C, 292M, 424M)
 - LMH0344 Triple-rate SDI Adaptive Cable Equalizer
 - LMH0340 Triple-rate SDI Serializer with integrated cable driver
 - LMH0341 Triple-rate SDI deserializer with reclocked loop through
 - LMH1981 Multi-Format Video Sync Separator
 - LMH1982 Multi-Rate Video Clock Generator
 - DS90CP22 2x2 LVDS Crosspoint Switch
 - LP3878 Adjustable Low Noise LDO
 - LM20242 PowerWise Buck Regulator
 - Interfaces directly to the Altera Video and Image Processing (VIP) Suite
- Collection of video reference designs



ViClaro II HD Video Enhancement Dev. Platform

microtronix Microtronix Datacom Ltd.

The Microtronix ViClaro II HD Video Enhancement Development Platform is targetted at the development of consumer HD video display and imaging systems. The ViClaro II incorporates an Altera Cyclone II FPGA to allow display designers and ASSP vendors to test next-generation picture enhancement features for their products and meets the needs of changing display technology, rather than being tied to lengthy application-specific integrated circuit (ASIC) development cycles.

Features

- 32-bit DDR2 SDRAM Memory
- HDMI Transmitter / Receiver
- Analog / Video Receiver
- Dual LVDS Links
- Supports 720p / 1080i / 1080p 50/60 Hz HDTV



ViClaro III Video Host Board

microtronix Microtronix Datacom Ltd.

The Microtronix ViClaro III HD Display Panel Video IP Development Kit is targetted at the development of consumer video display and imaging systems. It is designed to demonstrate the capabilities of Altera's Cyclone III for video and image enhancements applications in Video Display Controller ASSP systems.

Features

- EP3C120F780C7N
- 256 Mbyte DDR2 SDRAM (32 Meg x 64)
- 4-Lane PCI Express PHY
- USB 2.0 PHY
- I2C interface port
- 3 High Speed Mezzanine Connectors (HSMC)



Dual Input HD-SDI Switcher Design Kit

microtronix Microtronix Datacom Ltd.

The Microtronix Dual Input HD-SDI Video Switcher Design Kit provides a hardware platform for developing SDI video processing systems using the Cyclone III FPGA.

Features

- Altera EP3C120 Cyclone™ III FPGA
- 2 x Gennum GS2961 3G/HD/SD-SDI SDI Receivers
- 1 x Gennum GS491B HD/SD/Graphics Clock and Timing Generator with GENLOCK
- 1 x Gennum GS2962 3G/HD/SD-SDI Serializer
- 1 x Analog Devices AD7393 SD/HD Video Encoder
- 2 x HD/SD-SDI inputs (75Ω BNC)
- 1 x HD/SD-SDI output (75Ω BNC)
- 1 x analog video:
- 75Ω BNC composite video output or
- YPbPr component video output
- RS-232 DB9 serial control port



Quad Link LVDS Interface HSMC Board

 **Microtronix Datacom Ltd.**

The Quad Link LVDS Interface HSMC Daughtercard supports receive and transmit LVDS links each consisting of 5 data channels and 1 clock for a total of 48 LVDS channels. The standard configuration of 20 Tx + 4 clk and 20 Rx + 2 clk, is capable of supporting LCD display panels up to 1080p at 100/120Hz. On-board LVDS termination resistors can be removed to convert receiver channels into transmitters as required to support 12 or 14-bit color applications.

Features

- Optimized for video applications
 - Single core provides both LVDS transmitter and receiver functions
 - Support for both 28-bit and 35-bit parallel data
 - Supports 1, 2 and 4 link configurations
- No transmit PLL clock fine tuning required



Gigabit Ethernet PHY / HDMI Transmitter HSMC Board

 **Microtronix Datacom Ltd.**

The Microtronix Gigabit Ethernet PHY and HDMI Transmitter HSMC Daughtercard adds functionality to the ViClaro III, the Altera EP3C120 Development Kit or other third party FPGA development boards with a HSMC header.

Features

- The Marvell 88E1111 Gigabit Ethernet PHY is fully compatible with Altera's Triple Speed Ethernet MAC IP.
- Deep Color 12-bit Deep Color HDMI 1.3 Transmitter using the Analog Devices ADV7510 video chip.
- HSMC compatible daughter card



DVI Receiver / Transmitter HSMC Board

 **Microtronix Datacom Ltd.**

The Microtronix DVI Receiver / Transmitter HSMC Board is designed to allow developers access to high-quality, high resolution video signals in their FPGA designs. It integrates both a DVI receiver and transmitter onto the same card giving the flexibility required by high resolution image processing systems. Card is shipped with source code examples.

Features

- Digital Visual Interface Compliant (DVI 1.1)
- Supports resolutions from VGA to UXGA (1600x1200 and 1920x1080 [1080p@60])
- 25 - 165 Mhz Pixel rates
- EDID data reading/writing
- Monitor detection through Hot-Plug
- 15Mbps Optical S-PDIF TX and RX for digital audio connectivity



HDMI Rx/Tx HSMC Board

 **Microtronix Datacom Ltd.**

The Microtronix HDMI Receiver / Transmitter HSMC Daughtercard interfaces a HDMI receiver and transmitter to your Altera FPGA development kit using the HSMC expansion connector. The receiver also supports an analog component video (YCbCr) interface.

Features

- Uses the Analog Device AD9889 HDMI Transmitter and AD9880B HDMI Receiver
- Analog YCrCb Video Receiver
- Supports 480i / 720p / 1080i / 1080p @ 50/60 Hz
- EDID data reading / writing
- Auto detection of monitor through Hot-Plug
- Altera compatible HSMC expansion connector



Lancelot VGA Controller IP Design Kit

 **Microtronix Datacom Ltd.**

Microtronix is proud to offer the innovative Lancelot VGA IP Design Kit solution for customers wanting to develop video IP based solutions. The Lancelot Kit comes complete with an IP core written in VHDL that can be synthesized for all Altera FPGA devices.

Features

- Display resolutions: 640 x 480, 800 x 600, 1024 x 768
- Displays up to 24-bit color
- 900 LE's
- Video & audio development board
- VGA IP Core reference design & demo
- Compatible with Microtronix Multi-port SDRAM IP Core



High Speed AD/DA FPGA Board

 **SIGLEAD, Inc.**

Features

- Stratix III & IV 1152 pin devices
- AD/DA Converter SMA Connector differential input/output
- ADC: 12 bit 550MSPS dual channel
- DAC: 16 bit 1GSPS dual channel
- 27.000MHz oscillator
- MCX input
- On-board PLL
- CMX differential (single end) output dual channel
- DDR2 SDRAM 240pin DIMM (Max 4GBytes)
- DVI Input/Output Max. UXGA (165MHz)
- Gigabit Ethernet controller (PCI bus)
- USB2.0 A Connector x2 & mini AB connector x1
- LVDS Connector input/output 10 pairs each Max 10Gbps
- USB Serial I/F
- Expansion port 80pin connector (40 user pins)

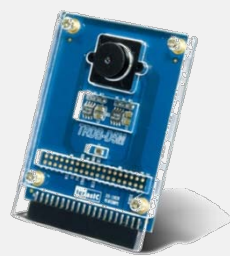


Altera DE4 Development and Education Board

terasic Terasic Technologies

Features

- Stratix IV GX EP4SGX230/EP4SGX530 with transceivers
- PCIe 2.0 x8 Connector and 2 DDR2 SO-DIMM
- 3 x USB ports (1 x mini AB host/device, 2 x type A host)
- SMA connectors for clocks and LVDS signals
- 4 x SATA connectors
- SD Card socket
- 64MB Flash (16-bit)
- 2MB ZBT SRAM
- I2C EEPROM
- 2 x HSMC connectors
- 2 sets of 40 pin Extension ports
- 50/100MHz Oscillator
- 4xGigabit Ethernet ports (4 x RJ-45)
- 4 x Push Button Switch, 4 x Slide Switch, 1 x 8-position DIP switch, 2 x 7-Seg, 8 x LEDs



5 Mega Pixel Digital Camera Package

terasic Terasic Technologies

Features

- Reference design with Verilog source code
- A User Manual with Live Demo examples
- Support exposure time controlling
- Support motion capture mode
- Software allows users to upload the picture captured into PC and save the picture into bitmap format or Joint Photographic Experts Group for viewing.
- Equipped with Micron 5 Mega Pixel CMOS sensor
- Support 2,592H x 1,944V active pixels
- Output data in RGB Bayer Pattern format
- Full resolution frame rate up to 15 frame per second (FPS)
- Provide users entire reference design (Frame Grabber, high-performance multi-port SDRAM frame buffer, image processing IPs)



SDI-HSMC Card

terasic Terasic Technologies

The Transceiver Serial Digital Interface (SDI) HSMC board provides a hardware platform for developing video broadcasting systems. It is intended to be used by customers to implement and design SDI and AES systems based on transceiver-based host boards with HSMC interface. It can also be part of an openly sold Development Kit, or bundled with packages of software and IP cores.

Features

- 2 SDI inputs and outputs
- 2 AES inputs and outputs
- SDI clean up PLL and an AES PLL
- Supports triple rate 3G/HD/SD SDI standard

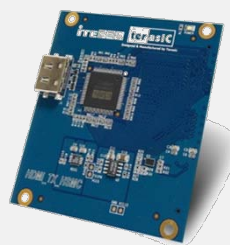


HDMI Receiver Daughter Card

terasic Terasic Technologies

HDMI_RX_HSMC is a HDMI receiver daughter board with HSMC (High Speed Mezzanine Connector) interface. The board contains the following rich features:

- One HSMC interface for connection purpose
- One HDMI receiver with dual receiving ports
- Two 2K EEPROM for storing EDID of two receiver ports separately
- Powered from 3.3V and 12V pins of HSMC connector



HDMI Transmitter Daughter Card

terasic Terasic Technologies

HDMI_TX_HSMC is a HDMI transmitter daughter board with HSMC (High Speed Mezzanine Connector) interface. The board contains the following rich features:

- One HSMC interface for connection purpose
- One HDMI transmitter with single transmitting port
- One 2K EEPROM
- Powered from 3.3V and 12V pins of HSMC connector



Vadex Box

Meganovo Meganovo Technologies Co Ltd

Features

- Tiler TILE36Pro or TILE64Pro
- Altera EP2AGX45 or EP2AGX65
- 6GB of SODIMM memory at 533MHz
- 2 1GigE interfaces
- 1 HDMI Out interfaces
- 1 VGA Out interfaces
- 1 BNC Out interfaces
- 1 HDMI In interfaces
- 2 Audio In and Out
- 1 PCI-e 4Lane for debug or extend
- Support H.264/MPEG4/MPEG2 decoder
- Support 1/4/6multi-picture, it also supports automatic switching of multi-picture with rolling
- Support 6 channel HD
- Support 1080P@30f,720P@30f,D1@30f
- Support RSTP/RSVP/FTP/HTTP/IGMP/NTP protocols
- It can seamless connect Telop server, insert Marquee

High Speed External Memory Interface Solutions

Altera's complete memory interface design solutions address today's high-speed memory interface challenges such as memory controller, I/O design, and board-level signal integrity issues. Altera's solutions include advanced device architectures, customizable MegaCore® functions, Quartus® II design software, reference designs, demonstration boards, and simulation models, accompanied by a rich set of technical documentation.

This table lists external memory interfaces supported by Altera FPGAs and HardCopy® ASICs.

Device	Memory Type						
	DDR3 SDRAM	DDR2 SDRAM	DDR SDRAM	RLDRAM II	RLDRAM III	QDR II SRAM	QDR II+ SRAM
Stratix V ⁽¹⁾	1,600 Mbps 800 MHz	800 Mbps 400 MHz	400 Mbps 200 MHz	800 Mbps 400 MHz	1,600 Mbps 800 MHz	1,400 Mbps 350 MHz	1,600 Mbps 400 MHz
Stratix IV	1,067 Mbps 533 MHz	800 Mbps 400 MHz	400 Mbps 200 MHz	800 Mbps 400 MHz	-	1,400 Mbps 350 MHz	1,600 Mbps 400 MHz
Stratix III	1,067 Mbps 533 MHz	800 Mbps 400 MHz	400 Mbps 200 MHz	800 Mbps 400 MHz	-	1,400 Mbps 350 MHz	1,600 Mbps 400 MHz
Stratix II and Stratix II GX	-	667 Mbps 333 MHz	400 Mbps 200 MHz	600 Mbps 300 MHz	-	1,200 Mbps 300 MHz	1,200 Mbps 300 MHz
Stratix and Stratix GX	-	-	400 Mbps 200 MHz	400 Mbps 200 MHz	-	800 Mbps 200 MHz	-
Arria V ⁽¹⁾	1,066 Mbps 533 MHz	800 Mbps 400 MHz	-	800 Mbps 400 MHz	-	1,400 Mbps 350 MHz	1,600 Mbps 400 MHz
Arria II GX	800 Mbps 400 MHz	667 Mbps 333 MHz	400 Mbps 200 MHz	-	-	1,000 Mbps 250 MHz	1,000 Mbps 250 MHz
Arria GX	-	466 Mbps 200 MHz	400 Mbps 200 MHz	-	-	-	-
Cyclone V ⁽¹⁾	1,066 Mbps 533 MHz	800 Mbps 400 MHz	-	800 Mbps 400 MHz	-	1,400 Mbps 350 MHz	1,600 Mbps 400 MHz
Cyclone IV	-	400 Mbps 200 MHz	333 Mbps 167 MHz	-	-	668 Mbps 167 MHz	-
Cyclone III LS	-	333 Mbps 167 MHz	300 Mbps 150 MHz	-	-	600 Mbps 150 MHz	-
Cyclone III	-	400 Mbps 200 MHz	333 Mbps 167 MHz	-	-	668 Mbps 167 MHz	-
Cyclone II	-	333 Mbps 167 MHz	333 Mbps 167 MHz	-	-	668 Mbps 167 MHz	-
HardCopy IV	1,067 Mbps 533 MHz	667 Mbps 333 MHz	400 Mbps 200 MHz	800 Mbps 400 MHz	-	1,200 Mbps 300 MHz	1,400 Mbps 350 MHz
HardCopy III	800 Mbps 400 MHz	667 Mbps 333 MHz	400 Mbps 200 MHz	667 Mbps 333 MHz	-	1,200 Mbps 300 MHz	1,400 Mbps 350 MHz
HardCopy II	-	533 Mbps 267 MHz	400 Mbps 200 MHz	500 Mbps 250 MHz	-	1,000 Mbps 250 MHz	1,000 Mbps 250 MHz

Note (1) Under characterization test.

DRAM Device Overview

DRAM devices are volatile memories offering a lower cost per bit than SRAM devices. A compact memory cell consisting of a capacitor and a transistor makes this possible over the six-transistor cell used in SRAM. However, the capacitor will discharge, causing the memory cell to lose its state, which means that DRAM memory needs to be refreshed periodically. Generally, you would choose SRAM devices for applications where latency or low interface complexity is important. You would choose DRAM where cost per bit is important. Special types of DRAM challenge this norm by offering improved random access latency, as well as a lower cost per bit.

Altera provides complete system solutions to help memory designers successfully interface Altera® FPGAs to a variety of DRAM devices.

DDR SDRAM

Double data rate (DDR) SDRAM is an evolution of single data rate (SDR) SDRAM. It offers higher performance through increased bus speeds using a lower I/O voltage (2.5 V), and most importantly, data transfer on both clock

edges, doubling the raw bandwidth. DDR SDRAM is a widely established memory technology. It offers the lowest cost per bit, due in part to its broad acceptance in almost any marketplace.

DDR3

DDR3 SDRAM is an improvement over its predecessor, DDR2 SDRAM. The primary benefit of DDR3 is the ability to transfer at twice the data rate of DDR2, thus enabling higher bus rates and higher peak rates than earlier memory technologies. In addition, the DDR3 standard allows for greater chip capacities. The

advantages of DDR3 architecture over DDR2 architecture are summarized as follows:

- Data rate speed ranges from 800 to 1,600Mbps
- Device capacity ranges from 512Mb to 8Gb
- Power is lower than DDR3 SDRAM due to reduced I/O and core voltage

DDR2 SDRAM

DDR2 SDRAM is an evolution of DDR SDRAM. It operates using a lower voltage (1.8V). DDR2 offers increased densities and even higher performance through higher bus speeds and an optimized interface. The advantages of DDR2 architecture over DDR architecture are summarized as follows:

- Data rate speed ranges from 400 to 667Mbps
- Power is lower than DDR SDRAM due to reduced I/O and core voltage
- Smaller footprint for FBGA packages

DDR

DDR SDRAM is an evolution of SDR SDRAM. It offers higher performance through increased bus speeds using a lower I/O voltage (2.5V), and most importantly, data transfer on both clock edges, doubling the raw bandwidth. DDR

SDRAM is a widely established memory technology. It offers the lowest cost per bit, due in part to its broad acceptance in almost any marketplace.

RLDRAM II

RLDRAM II is the second generation of RLDRAM. It is a development of DDR SDRAM, designed to address the low latency requirements of certain applications, such as packet buffers in high-performance line cards. RLDRAM II has a high-performance DDR data bus and offers a non-multiplexed address bus,

reducing the number of clock cycles to initiate read or write applications. A banked architecture also reduces access time. In some systems, RLDRAM II eliminates the need for specialized content-addressable memory (CAM) or SRAM.

RLDRAM III

RLDRAM III is the third generation of RLDRAM. It is a development of DDR SDRAM, designed to address the low latency requirements of certain applications, such as packet buffers in high-performance line cards. RLDRAM III has a high-performance DDR data bus and offers a non-multiplexed address bus,

reducing the number of clock cycles to initiate read or write applications. A banked architecture also reduces access time. In some systems, RLDRAM III eliminates the need for specialized content-addressable memory (CAM) or SRAM.

SDR DRAM

SDR SDRAM is the first generation of synchronous DRAM. It improves memory bandwidth over extended data out (EDO) DRAM

by offering data transfer up to once-per-clock cycle.

SRAM Device Overview

Altera provides a complete system solution to help you successfully interface Altera® FPGAs and HardCopy® ASICs to a variety of SRAM devices. SRAM devices offer extremely fast access times — approximately four times faster than DRAM — but are much more expensive to produce. Unlike DRAM, SRAM does not need to be refreshed periodically to prevent data loss through leakage. SRAM devices are capable of storing data as long as the device is supplied with power. If the power is turned off, the contents are lost. Typical systems require both SRAM (for performance-critical applications) and DRAM memory (for all other applications).

QDR and QDR II SRAM Devices

QDR memory devices allow two ports to run independently at DDR, which results in four data items per clock cycle. QDR SRAMs enable you to maximize bandwidth by allowing operation at data rates above 200MHz. The QDR

architecture allows you to reach these speeds without the possibility of bus contention.

The QDR consortium, which consists of Cypress Semiconductor, Integrated Device Technology (IDT), Micron Technology, and NEC Corporation,

developed the QDR architecture. QDR is designed to meet the high-performance needs of

high-speed networking applications.

ZBT SRAM Devices

ZBT SRAM is a synchronous burst SRAM with a simplified interface that provides higher bandwidth and efficient bus utilization by eliminating turnaround cycles and idle cycles

between read and write operations. IDT, Micron, and Motorola jointly developed the ZBT SRAM architecture, which is optimized for networking and telecommunications applications.

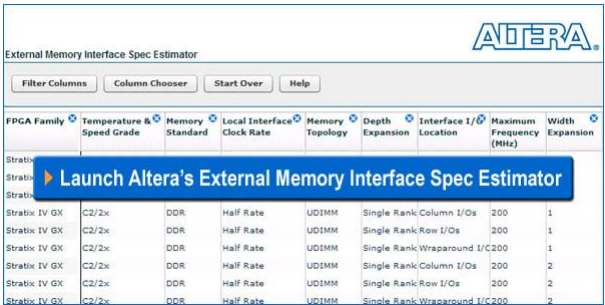
External Memory Interface Spec Estimator

Altera’s External Memory Interface Spec Estimator, a parametric tool, allows you to find and compare the supported external memory interfaces’ highest performance in our FPGA devices. You’ll have the ability to filter down to specific performances based on your own search specifications, and then compare performances across FPGA devices side-by-side by filtering the criteria you choose for analysis. The External Memory Interface Spec Estimator supports DDR3 SDRAM, DDR2 SDRAM, DDR SDRAM, RLDRAM II, QDRII+ SRAM, and QDRII SRAM interfaces.

The stated performances are the maximum clock rates supported in Altera’s FPGA devices based on the listed features across supported high speed memory standards.

The maximum clock rates are only estimates based on a standalone Altera ALTMEMPHY or UniPHY and High-Performance Controller II instance generated with the default PHY and controller parameters in the MegaCore® IP. For the actual performance of your design, you must always compile and timing-analyze your complete design in the Quartus® II software.

The External Memory Interface Spec Estimator replaces the maximum clock rate tables in Volume 1 Section III: “System Performance Specifications” of the External Memory Interfaces Handbook. The FPGA devices supported by the External Memory Interface Spec Estimator are the Stratix® V, Stratix IV, Stratix III, Arria® II GX, Cyclone® IV, and Cyclone III device families.



External Memory Interface Board Solutions

Stratix IV E FPGA Development Kit



ALTERA Altera Corporation

The Altera Stratix IV GX FPGA Development Kit delivers a complete system-level design environment that includes both the hardware and software needed to immediately begin developing FPGA designs. With this PCI-SIG- compliant board and a 1-year license for Quartus II design software, you can:

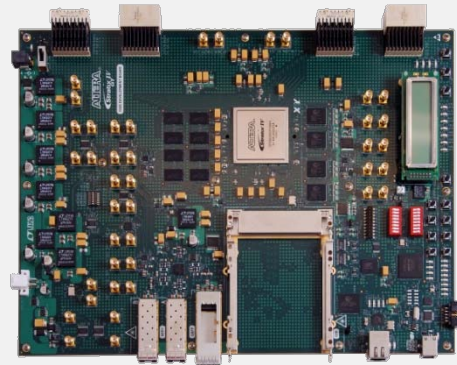
- Develop and test PCI Express 2.0 (up to x8 lane) endpoint and rootpoint designs
- Develop and test memory subsystems consisting of DDR3 and/or QDR II+ memory
- Build designs capable of migrating to Altera's low-cost HardCopy IV ASICs.

Features

- Altera Stratix IV GX EP4SGX230KF40C2N
- On-board clock oscillators
 - SMA connectors for external clock input /output
- General user input/output
 - LEDs & LCD display
 - Push-button & DIP switches
- **DDR3 SDRAM** 512-MByte (64-bit data) & 128-MByte (16-bit data)
- 4-MByte **QDR II+ SRAMs** (18-bit data) x 2 pcs
- 64-MByte **Sync Flash** & 2-MByte **SSRAM**
- PCI Express x8 edge connector
- 10/100/1000BASE-T Ethernet PHY with RJ-45 connector

- Two HSMC connectors
- HDMI video output 3G SDI video input and output
- Power & Temperature measurement circuitries
- Other features
 - Stratix IV GX FPGA Development Kit CD-ROM
 - Design Examples
 - Board Update Portal featuring the Nios II processor web server and remote system update Board Test System
 - Complete documentation
 - Altera's Complete Design Suite DVD
 - MegaCore IP Library includes PCI Express, Triple-Speed Ethernet, SDI, and DDR3 High-Performance Controller MegaCore IP cores

Stratix IV GT 100G Development Kit



ALTERA Altera Corporation

The Altera Stratix IV GT 100G Development Kit delivers a platform that can be used to implement 100 Gigabit serial data communications systems. Stratix IV GT FPGAs are optimized specifically for the latest generation of 40G and 100G applications used in communications systems, high-end test equipment and military communications systems. The 11.3-Gbps integrated transceivers featured in the Stratix IV GT FPGA provide customers a true single-FPGA 100G solution, enabling 100G optical modules to interface directly with the FPGA. This board will accommodate two SFP+ optical modules (one with EDC and one without (not included in the kit)), a 4 lane QSFP optical module (not included in

the kit), a CFP interface, and a 20 lane Interlaken interface.

Features

- Altera Stratix IV GT EP4S100G5F1932
- Configuration
 - Embedded USB Blaster
 - 1G flash device (FPP via System Controller MAX II Device)
- Memory Interfaces
 - Two **DDR3** interfaces, x32 bit data buses
 - ✧ Tree topology; simultaneous operation to 400MHz
 - ✧ Should be able to run one at 533 MHz

- Four **QDR II** interfaces x18 bit data buses
 - ✧ 400MHz
- Components and Interfaces
 - 10 Transceivers to CFP
 - 2 Transceiver to SFP+ (one w/EDC, one w/o)
 - 4 Transceivers to QSFP
 - 20 Transceivers to FCI Airmax (Interlaken)
 - 10/100/1000Mbps Ethernet with RJ-45
- Power & temperature measurement circuitry

Board Solutions from Third Party Board Partners

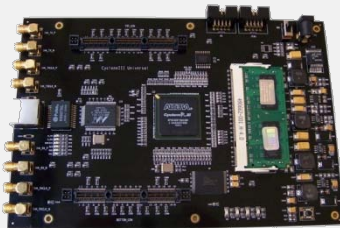


**ALL-IN-ONE Base Board B-11
(Stratix III Edition)**

 **Accverinos Co.,Ltd.**

Features

- EP3SL340F1517 or EP3SL200F1517 (-2 or -3)
- DDR2 DIMM
- DVI I/O Support: 1 each of input and output port using TI TFP403 & 410 chips. Guaranteed to operate at 165MHz
- 1 x Gigabit Ethernet PHY & RJ45 Connector.
- 1 x USB2.0 Connector, Cypress EZ-USB and ULPI supporting PHY · Can use either of USB MCU or PHY
- 8 pairs each of input and output signals through C44LVDS connectors. Tested 1.2Gbps/pair operation
- SD Card support (connected directly to FPGA and controlled by MegaCore IP)
- 1 x Altera standard HSMC connector
- 5 x Samtec 120-pin connectors



CycloneIII SOPC board

 **Hangzhou Free Electron Co. Ltd**

This board offer Ethernet, DDR2 interface, enough test port and expend IO. It is suitable for SOPC system design and small/middle density IP/ASIC verification.

Features

- Cyclone III EP3C80F780C8N or EP3C120F780C8N
- 256MB DDR2 SO-DIMM (up to 2GB)
- 12 layer PCB
- 216 expand IO/CLK/PLLOUT (include 9 lvds in,lvds out)
- Marvel 10M/100M/1000MEathernet PHY
- SMA clock/data input/output
- 32M FLASH
- 4 LED, one reset

High Speed Interface Solutions

Transceiver Portfolio

Altera is a pioneer and leader in integrating transceivers into FPGAs. In 2001, we introduced our first FPGA family with integrated transceivers. Since then, we've introduced many innovations to make transceivers run faster, operate more reliably, and support emerging protocols with each generation of FPGAs and ASICs. With a top-notch, in-house transceiver design team, we're equipped to continue tailoring transceivers for specific applications.

At 28 nm, our latest transceiver-related innovations include:

- Technology for 12.5-Gbps and 28-Gbps transceivers
- Support for driving optical modules directly with built-in:
 - ✧ Electronic dispersion compensation (EDC)
 - ✧ LC- (inductor-capacitor) based phase-locked loops (PLLs) for ultra low jitter
- Support for driving 10G backplanes directly with:
 - ✧ Transmitter pre-emphasis
 - ✧ Receiver 5-tap distributed feedback equalizer (DFE)
 - ✧ Receiver 4-stage continuous time linear equalization (CTLE)
 - ✧ Plug & Play Signal Integrity with adaptive dispersion compensation engine (ADCE)
- Full-featured physical coding sub-layer (PCS) including:
 - ✧ 8b/10b encoder/decoder
 - ✧ 64/66 encoder/decoder
 - ✧ Gearbox
 - ✧ Channel bonding
- Support for PCI Express Gen1/2/3 and FPGA configuration through PCI Express
- Support for 40G and 100G data path
- On-chip instrumentation with EyeQ horizontal and vertical data eye monitor
- Dynamic and fine-grained partial reconfiguration

- Extensive intellectual property (IP) library of industry-standard transceiver protocols

Device	Maximum Number of Channels	Maximum Data Rate (Gbps)	Backplane Support	Optical Module Support
Stratix V GT (28 nm)	66	12.5	Yes	Yes
Stratix V GX (28 nm)	66	8.5	Yes	Yes
Stratix IV GT (40 nm)	48	11.3	Yes	Yes
Stratix IV GX (40 nm)	48	8.5	Yes	Yes
HardCopy® IV GX (40 nm)	36	6.5	Yes	Yes
Arria® II GZ (40 nm)	24	6.375	Yes	Yes
Arria II GX (40 nm)	16	6.375	-	-
Cyclone IV GX (60 nm)	8	3.125	-	-

Altera provides a broad portfolio of FPGAs and ASICs with integrated transceivers to address bandwidth needs from consumer to wireline applications. Within this portfolio, you'll discover a diverse mix of FPGAs and ASICs with as many as 66 28-Gbps backplane transceiver channels in Stratix® V GT FPGAs to as few as two 3.125-Gbps transceiver channels in Cyclone® IV GX FPGAs to fit your system needs. See the table above for more details about our wide breadth of FPGAs and ASICs with integrated transceivers.

The portfolio also offers the productivity advantage of the comprehensive Quartus® II

design software, a common set of IP cores, sophisticated signal integrity tools, and a variety of supporting reference designs and design examples. Learn the software once, then extend your skills across multiple design platforms.

With the transceiver device and Quartus II design software, you'll experience:

- Faster design and compile times

- More efficient system resource utilization resulting in higher system integration
- Higher integration with higher density products
- Optimized core performance, so you can efficiently close timing on designs and lower your engineering costs
- The ability to seamlessly connect IP blocks with a simple, intuitive GUI

Protocol Solutions

Altera® FPGAs and HardCopy® ASICs with integrated transceivers offer a range of data rates to suit all applications from 600 Mbps to 28 Gbps.

Protocol	Stratix® Series FPGAs			HardCopy ASICs			Arria® Series FPGAs	Cyclone® Series FPGAs
	V GX/GS	V GT	IV GX	IV GT	V GX	IV GX	II GX	IV GX
3G-SDI	✓	✓	✓	✓	✓	✓	✓	✓
10G-SDI	✓	✓	-	✓	✓	-	-	-
10 Gigabit Ethernet XAUI	✓	✓	✓	✓	✓	✓	✓	✓
ASI	✓	✓	✓	✓	✓	✓	✓	-
Basic Mode	✓	✓	✓	✓	✓	✓	✓	✓
CEI-6G/SR/LR	✓	✓	✓	✓	✓	✓	-	-
CEI-11G/SR/LR	✓	✓	-	✓	✓	-	-	-
CPRI	✓	✓	✓	✓	✓	✓	✓	✓
DDR-XAUI	✓	✓	✓	✓	✓	✓	-	-
DisplayPort	-	-	-	-	-	-	-	✓
Fibre Channel	✓	✓	✓	✓	✓	✓	-	-
Gigabit Ethernet	✓	✓	✓	✓	✓	✓	✓	✓
GPON	✓	✓	✓	✓	✓	✓	✓	-
HiGig+	✓	✓	✓	✓	✓	✓	✓	-
HiGig2	✓	✓	✓	✓	✓	✓	-	-
HyperTransport 3.0	✓	✓	✓	✓	✓	✓	-	-
IEEE 802.3ae 10GBase-R	✓	✓	-	✓	✓	-	-	-
IEEE 802.3ba 10GBase-KR	✓	✓	-	-	✓	-	-	-
IEEE 802.3ba 40G	✓	✓	-	✓	✓	-	-	-

Protocol	Stratix® Series FPGAs			HardCopy ASICs			Arria® Series FPGAs	Cyclone® Series FPGAs
	V GX/GS	V GT	IV GX	IV GT	V GX	IV GX	II GX	IV GX
IEEE 802.3ba 100G	✓	✓	-	✓	✓	-	-	-
Interlaken	✓	✓	✓	✓	✓	✓	-	-
Interlaken (10G)	✓	✓	-	✓	✓	-	-	-
JESD204A	✓	✓	✓	✓	✓	✓	✓	✓
OBSAI	✓	✓	✓	✓	✓	✓	✓	✓
OTU-2 (G.709)	✓	✓	-	✓	✓	-	-	-
OTU-3	✓	✓	-	✓	✓	-	-	-
OTU-4	✓	✓	-	✓	✓	-	-	-
PCI Express Gen1	✓	✓	✓	✓	✓	✓	✓	✓
PCI Express Gen2	✓	✓	✓	✓	✓	✓	-	-
PCI Express Gen3	✓	✓	-	-	✓	-	-	-
QDR InfiniBand	✓	✓	-	-	✓	-	-	-
QPI	✓	✓	-	-	✓	-	-	-
SAS	✓	✓	✓	✓	✓	✓	✓	-
SATA	✓	✓	✓	✓	✓	✓	✓	✓
SDI SD/HD	✓	✓	✓	✓	✓	✓	✓	✓
SerialLite II	✓	✓	✓	✓	✓	✓	-	-
Serial RapidIO®	✓	✓	✓	✓	✓	✓	✓	✓
SFP+	✓	✓	-	✓	✓	-	-	-
SFI-4.2	✓	✓	✓	✓	✓	✓	✓	-
SFI-5.1	✓	✓	✓	✓	✓	✓	-	-
SFI-5.2	✓	✓	-	✓	✓	-	-	-
SGMII	✓	✓	✓	✓	✓	✓	-	-
SONET OC-3/OC-12/OC-48	✓	✓	✓	✓	✓	✓	✓	-
SONET OC-192	✓	✓	-	✓	✓	-	-	-
SPI-4.2	✓	✓	✓	✓	✓	✓	✓	✓
SPI-5.1	✓	✓	✓	✓	✓	✓	✓	-
SPAUI	✓	✓	✓	✓	✓	✓	-	-
V-by-One	-	-	-	-	-	-	-	✓
XFP	✓	✓	-	✓	✓	-	-	-

Plug & Play Signal Integrity

Available in Stratix® and Arria® series FPGAs and HardCopy® ASICs with integrated multi-gigabit transceivers, Plug & Play Signal Integrity lets you change the position of backplane cards on the fly while eliminating the painstaking process of manually reconfiguring your backplane equalization settings

With this capability, you can design systems with truly universal cards that plug into multiple card positions in system backplanes (as shown in this picture in the right. Altera's hot-socketable transceivers, coupled with adaptive dispersion compensation engine (ADCE) technology, deliver Plug & Play Signal Integrity where the same card configuration can be used, irrespective of slot position in most systems.

In our 28-nm Stratix V FPGAs, the adaptive engine extends beyond linear equalization. When operating high-speed serial links in noisy environments, the benefits of the 5-tap decision feedback equalization (DFE) mitigates the effects of cross-talk to ensure high reliability of a system with a low bit-error ratio (BER).

Plug & Play Signal Integrity offers wide-ranging benefits:



- Reduced card-type inventories
- Increased system flexibility
- Reduced maintenance and training costs
- Simplified order code management
- Reduced effort in the lab, since you no longer need to characterize every card slot to determine the optimal signal integrity setting for each one.

When you design with Altera, you can design with the confidence that variations (in manufacturing, materials, temperature, voltage, and silicon process) are continuously monitored and compensated for by the ADCE to deliver the best eye opening and system BER performance.

High Speed Interface Board Solutions

Transceiver Signal Integrity Development Kit, Stratix IV GT Edition



ALTERA Altera Corporation

Altera's Transceiver Signal Integrity Development Kit, Stratix IV GT Edition enables a thorough evaluation of transceiver interoperability and serializer/deserializer (SERDES) signal integrity by allowing you to evaluate transceiver performance up to 11.3 Gbps (Altera Stratix IV P4SGX230KF40C2N)

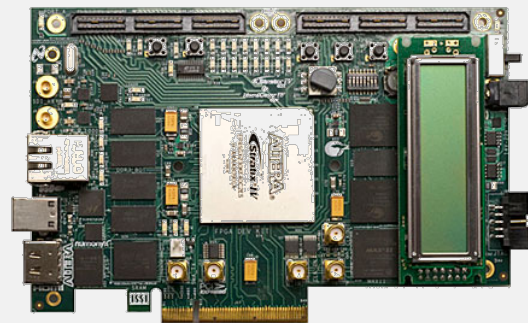
Features

- Stratix IV GT development board
- EP4S100G2F40I1N
- On-board clock oscillators: 50 MHz, 100 MHz, 644.53 MHz, and 706.25 MHz
- SMA connectors for supplying an external differential clock to transceiver reference clock

- DIP and push-button switches
- LEDs
- LCD
- 64-MB sync flash memory (primarily to store FPGA configurations)
- Six full-duplex transceiver channels routed to SMA connectors
 - All channels support up to 11.3-Gbps data rate
- Six full-duplex transceiver channels routed to FCI Airmax connector
- Power measurement circuitry on transceiver-related supplies
- The voltage on all (and only) these rails can be supplied via banana jacks
- Temperature measurement circuitry

- RJ-45 jack and 10/100/1000Base-T Ethernet PHY
- Backplane drive capability at 6.5 Gbps
- Directly connect the transceiver signal integrity development kit to an FCI backplane (not included) through the FCI connector header
- Couple with a second signal integrity development kit or FCI daughtercard (not included) for a complete end-to-end backplane channel analysis
- Application GUI
- Platform independent
- Interfaces to PC via JTAG
- Embedded blaster
- Quartus II software license is not included and is not required for kit evaluation

Stratix IV GX FPGA Development Kit



ALTERA Altera Corporation

The Altera Stratix IV GX FPGA Development Kit delivers a complete system-level design environment that includes both the hardware and software needed to immediately begin developing FPGA designs. With this PCI-SIG-compliant board and a 1-year license for Quartus II design software, you can:

- Develop and test PCI Express 2.0 (up to x8 lane) endpoint and rootpoint designs
- Develop and test memory subsystems consisting of DDR3 and/or QDR II+ memory
- Build designs capable of migrating to Altera's low-cost HardCopy IV ASICs.

Features

- Stratix IV GX FPGA development board
- Stratix IV GX FPGA EP4SGX230KF40C2N
- On-board clock oscillators
- SMA connectors for external clock input & output
- LEDs & LCD display
- Push-button & DIP switches
- DDR3 SDRAM
 - 512-MByte (64-bit data)
 - 128-MByte (16-bit data)
- 4-MByte QDR II+ SRAMs (18-bit data) x 2 pcs
- 64-MByte Sync Flash & 2-MByte SSRAM
- PCI Express x8 edge connector
- 10/100/1000BASE-T Ethernet PHY with RJ-45 connector

- Two HSMC connectors
- HDMI video output
- 3G SDI video input and output
- Power & Temperature measurement circuitries
- Stratix IV GX FPGA Development Kit CD-ROM
- Design Examples
- Board Update Portal featuring the Nios II processor web server and remote system update
- Board Test System
- Complete documentation
- Altera's Complete Design Suite DVD
- MegaCore IP Library includes PCI Express, Triple-Speed Ethernet, SDI, and DDR3 High-Performance Controller MegaCore IP cores

Arria II GX FPGA Development Kit



ALTERA Altera Corporation

The Altera Arria II GX FPGA Development Kit delivers a complete system-level design environment that includes both the hardware and software needed to immediately begin developing FPGA designs. With this PCI-SIG-compliant board and a one-year license for Quartus II design software, you can:

- Develop and test PCI Express 1.0 (up to x8 lane) designs
- Develop and test memory subsystems consisting of DDR2 and/or DDR3 memory
- Develop and test designs based on other Arria II GX supported protocol interfaces such as Gigabit Ethernet, SDI, CPRI, OBSAI, SAS/SATA, and Serial RapidIO.

Features

- Arria II GX EP2AGX125EF35 FPGA
- On-board ports
 - One HSMC expansion port
 - One gigabit Ethernet port
- On-board memory
 - 128-MB 16-bit DDR3 device
 - 1-GB 64-bit DDR2 SODIMM
 - 2-MB SSRAM
 - 64-MB flash
- On-board clocking circuitry
 - Four on-board oscillators
 - 100 MHz

- Programmable oscillator, default frequency 125 MHz
- Programmable oscillator, default frequency 100 MHz
- 155.52 MHz
- SMA connectors for clock input/output
- General user I/O
 - LEDs/displays

Cyclone IV GX Transceiver Starter Kit



ALTERA Altera Corporation

Altera's Cyclone® IV GX Transceiver Starter Kit provides a low-cost platform for developing transceiver I/O-based FPGA designs. This kit includes the complete hardware and software for you to:

- Develop your FPGA design for cost-sensitive applications
- Measure the FPGA's low power consumption
- Test signal quality of the FPGA transceiver I/Os (up to 2.5 Gbps)
- Develop and test PCI Express® 1.0 endpoint x1 lane designs (~250-Mbps transfer rate)

Features

- Cyclone IV GX transceiver starter board

- Cyclone IV GX EP4CGX15BF14C8N FPGA
- MAX® II CPLD EPM2210 System Controller enabling passive serial (PS) configuration from flash
- Embedded USB-Blaster™ for using the Quartus II Programmer
- JTAG header for external USB-Blaster
- Altera EPCS serial configuration device
- FPGA clock sources: 50 MHz, 125 MHz, and SMA clock input
- Other on-board oscillators: 6 MHz, 24 MHz, and 25 MHz
- LEDs
- Two-line character LCD display
- Push-buttons

- 16 MB of flash
- 2 MB of synchronous SRAM
- PCI Express edge connector
- 10/100/1000BASE-T Ethernet PHY with RJ-45 connector or one transceiver to SMA connectors (requires a minor board modification)
- On-board power measurement circuitry
- Laptop DC input
- PCI Express edge connector
- Power management solution from Linear Technology
- PCI Express low-profile (6.6" x 2.713") board form factor

Board Solutions from Third Party Board Partners



3FAD/D4-AMC



BittWare, Inc.

Dual Altera Stratix® IV FPGA AdvancedMC with 1 to 4 channels 8-bit, up to 5 GSPS ADC

Features

- 1 - 4 Channels 8-bit, up to 5 GSPS ADC
- Dual FPGAs: Altera Stratix IV E and Stratix IV GX supported by BittWare's ATLANTiS™ FrameWork
- BittWare's FINE™ III Host/Control Bridge provides control plane processing and interface
- AMC I/O: 18 ports SerDes, 1 port GigE
- Additional I/O: 10/100 Ethernet, 16 GPIO, RS-232, and JTAG



3FDJ/D4-AMC

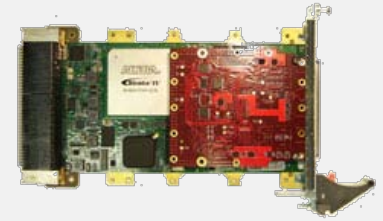


BittWare, Inc.

Dual Altera Stratix® IV FPGA AdvancedMC with 1 or 2 channels 16-bit, up to 1 GSPS DAC

Features

- 1 - 4 channels 16-bit, up to 1 GSPS DAC
- Dual FPGAs: Altera Stratix IV E and Stratix IV GX supported by BittWare's ATLANTiS™ FrameWork
- BittWare's FINE™ III Host/Control Bridge provides control plane processing and interface
- AMC I/O: 18 ports SerDes, 1 port GigE
- Additional I/O: 10/100 Ethernet, 16 GPIO, RS-232, and JTAG



3FAD/S4-3U-VPX



BittWare, Inc.

Commercial & Rugged Altera Stratix® IV GX 3U VPX Board with 1 to 4 channels 8-bit, up to 5 GSPS ADC

Features

- 1 - 4 Channels 8-bit, up to 5 GSPS ADC
- High density Altera Stratix IV GX supported by BittWare ATLANTiS™ FrameWork for FPGAs
- BittWare FINE™ Host/Control Bridge provides control plane processing and interface
- Fully connected to VPX: GigE, 15 SerDes, 32 LVDS
- Additional I/O: 10/100 Ethernet, RS-232, JTAG



3FAD/S4-AMC



BittWare, Inc.

Altera Stratix® IV GX AdvancedMC with 1 to 4 channels 8-bit, up to 5 GSPS ADC

Features

- 1 - 4 Channels 8-bit, up to 5 GSPS ADC
- High density Altera Stratix IV GX supported by BittWare's ATLANTiS™ FrameWork
- BittWare's FINE™ III Host/Control Bridge provides control plane processing and interface
- Fully connected to AMC (16 ports SerDes, 4 ports LVDS)

I/O includes 10/100/1000 Ethernet, SerDes, LVDS, RS-232, and JTAG



D4-AMC

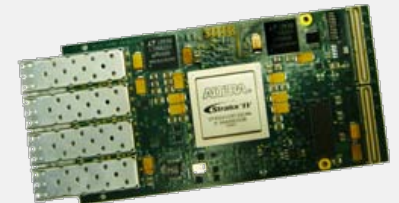


BittWare, Inc.

Dual Altera Stratix® IV FPGA AdvancedMC with VITA 57 Site

Features

- VITA 57 FMC site for I/O and processing expansion
- Dual FPGAs: Altera Stratix IV E and Stratix IV GX supported by BittWare's ATLANTiS™ FrameWork
- BittWare's FINE™ III Host/Control Bridge provides control plane processing and interface
- AMC I/O: 18 ports SerDes, 1 port GigE
- Additional I/O: 10/100 Ethernet, 16 GPIO, RS-232, and JTAG



4S-XMC



BittWare, Inc.

Altera Stratix® IV GX XMC with 4 SFP Transceivers

Features

- High density Altera Stratix IV GX FPGA
- 4 SFP transceivers on front panel
- 8 multi-gigabit serial transceivers
- On-board oscillators for Fibre Channel, PCI Express, and Serial RapidIO
- 44 general purpose digital I/O



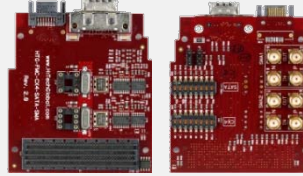
Altera Stratix IV GX/GT PCI Express Gen 2 / USB 3.0 / SFP+ Development Platform



HiTech Global, LLC

Features

- Altera Stratix 4GX EP4SGX230, 290, 360, 530, and 4GT EP4S100G2
- x8 PCI Express Gen 2 end-point (40 Gbps)
- DDR3 SO-DIMM (up to 4 GB)
- 256 MB DDR2
- x2 SFP+ with Netlogic AEL2006 dual Physical layer retimer with an integrated Electronic Dispersion Compensation (EDC) engine
- x2 Gigabit Ethernet
- USB 3.0 / 2.0 Host (5.0 Gbps) & Device (5.0 Gbps)
- x16 SMA (for 4 Serial Transceiver Ports) with external clock interface (connected to 10Gig transceivers with the GT model).
- High-speed Expansion Connector with 8 data-rate-adjustable Serial Transceivers and LVDS signals
- x8 rate-adjustable Serial Transceivers (SerDes)



Back / Front

HTG-FMC-CX4-SATA-SMA

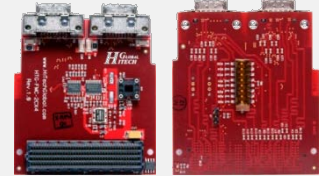


HiTech Global, LLC

FMC daughter card with one CX4, two SATA, and two SMA ports

Features

- CX4 Connector (x1)
- SATA (x2)
- SMA (x8 for two Serial Transceivers)
- Frequency Synthesizer (x2)
- Clock Buffer (x2)
- EEPROM
- FMC Connector



Back / Front

HTG-FMC-2CX4

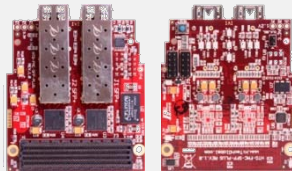


HiTech Global, LLC

FMC daughter card with two CX4 connectors providing access to two 10Gig ports

Features

- CX4 Connector (x2)- Provides access to total of 8 Serial Transceivers
- Frequency Synthesizer (x2)
- Clock Buffer
- EEPROM
- FMC Connector



Back / Front

HTG-FMC-SFP-PLUS

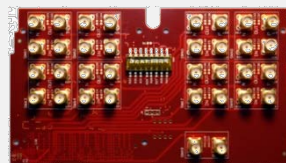


HiTech Global, LLC

FMC daughter card with two SFP+ connectors, two 10Gbps physical layer transceivers which provide full PCS, PMA, and XGXS sub-layer functionality

Features

- SFP+ Connector (x2)
- EEPROM
- FMC Connector
- On-board clock



HTG-FMC-X8SMA

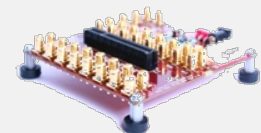


HiTech Global, LLC

FMC daughter card with 32 SMA connectors for 8 serial transceiver ports, two SMA connectors for external clock, and on-board super clocks

Features

- x32 SMA FMC Module- Provides access to total of 8 Serial Transceiver Ports
- Frequency Synthesizer and 3 different oscillators sources
- SMA connectors for external differential clocks
- Clock Buffer
- EEPROM
- FMC Connector



HTG-PCIE-TEST



HiTech Global, LLC

This module can be used for:

- PCI Express Test - Provides incoming clocks ranging from 100MHz to 250MHz and power (12V and 3.3V) for quick electrical verification of any PCI Express card (Gen1 and 2).
- PCI Express Loopback Test - PHY or Serial Transceivers used as PHY can be tested for functionality and performance
- Serial Transceiver Expansion - Serial Transceivers used as PCIe PHY can be used for other serial interfaces through SMA cables

Features

- x8 PCI Express Gen1 and Gen2 Female Connector
- Super clock generating 100MHz, 250MHz and other related frequencies
- External Clock Outputs
- Breakout SMA Connectors for Tx and Rx lanes

Embedded System Design Solution

Why Use FPGAs in Embedded Designs?

Altera's powerful development tools let you create custom systems on a programmable chip, making FPGAs the platform of choice. When you think embedded, think FPGAs, think Altera. Here's why:



- **Increase productivity**
Whether you are a hardware designer or software developer, we have tools to provide you with unprecedented time and cost savings.
- **Protect your software investment from processor obsolescence**
Altera's embedded solutions protect the most expensive and time consuming part of your embedded design — the software.
- **Scale system performance**
Increase your performance at any phase of the design cycle by adding processors, custom instructions, hardware accelerators, and leverage the inherent parallelism of FPGAs.
- **Reduce cost**
Reduce your system costs through system-level integration, design productivity, and a migration path to high-volume HardCopy® ASICs.
- **Establish a competitive advantage with flexible hardware**
Choose the exact processor and peripherals for your application. Deploy your products quickly, and feature-fill over time to accelerate your time-to-market and establish a competitive advantage.

What Do I Need to Know to Get Started?

Evaluate our tools and develop software for free. When you are ready to ship your product, you must purchase a Nios® II intellectual property (IP) core license. This royalty-free license never expires and allows you to target your processor design to any Altera® FPGA, so your software investment is preserved even if the underlying

hardware changes. Follow the steps below to get started today:

1. Get the Design Software
2. Evaluate the Software and Develop the Application
3. Purchase Licensing

Step 1: Get the Design Software

There are several ways to get the Nios II processor and Nios II EDS development tools:

Web download—All the software tools you need to start development are available for immediate download: the Quartus® II design software, the Nios IDE, and the SOPC Builder system development software. Download software from the Altera site.

Development kits—Nios II development kits include a hardware development board,

download cables, reference designs, a perpetual-use royalty-free license for the Nios II processor, and all the design software you need to begin designing embedded systems for FPGAs.

Altera subscription—If you already have an Altera software subscription, you automatically receive all of the design software you need with each release.

Product	Web Download	Development Kit	Altera Software Subscription
Nios II Processor IP	✓ (1)	✓	✓ (1)
Nios II Embedded Development Suite	✓	✓	✓
NicheStack TCP/IP Network Stack, Nios II Edition	✓ (1)	✓ (1)	✓ (1)
Micrium MicroC/OS-II RTOS	✓ (1)	✓ (1)	✓ (1)
Nios II C2H Compiler	✓ (1)	✓ (1)	✓ (1)
Quartus II FPGA Design Software	✓	✓	✓
SOPC Builder System Development Software	✓	✓	✓
ModelSim® Altera Edition	-	✓	-
ModelSim Altera Web Edition	✓	-	-
JTAG Download Cable	-	✓	-
Development Board	-	✓	-

Note: 1. License sold separately.

Step 2: Evaluate the Software and Develop the Application

Build your applications and evaluate the Nios II embedded design flow.

Design, compile, and generate time-limited Nios II processor systems and hardware accelerators generated by the Nios II C-to-Hardware (C2H) Acceleration Compiler without obtaining a license file by using the OpenCore Plus evaluation feature.

Many reference designs and tutorials are included with the Nios II Embedded Design

Suite. Additionally, training is available on the web and in instructor-led courses.

You do not need a license if you are only developing software using the Nios II Embedded Design Suite. Before shipping a product containing one or more Nios II processors or accelerators generated by the Nios II C2H Compiler, you must purchase a license.

Step 3: Purchase Licensing

Purchase a license for the Nios II processor IP core and related products.

Nios II IP Core and Related Products

Nios II Processor IP

Get a license file for the Nios II processor, non-time-limited use, by purchasing a Nios II development kit or the stand-alone Nios II processor core license (ordering code: IP-NIOS).

Both fixed and floating licenses are available. To obtain a license file, contact your local Altera representative or Altera Tools Support.

Nios II C2H Compiler

To license the Nios II C2H Compiler, you need an active Nios II processor license. To obtain licenses for the Nios II C2H Compiler (ordering

code: IPT-C2H-NIOS) contact your local Altera representative or Altera Tools Support.

NicheStack TCP/IP Network Stack—Nios II Edition

To purchase a license for the NicheStack TCP/IP Network Stack, Nios II Edition, (ordering code:

IPSW-TCPIP-NIOS) contact your local Altera representative or Altera Tools Support.

Micrium MicroC/OS-II RTOS

To obtain a license for the Micrium MicroC/OS-II RTOS, contact Micrium today.

The Nios II processor is supported by a wide range of embedded software partners. Learn more about our embedded software partners.

Development Tools

Altera offers a variety of development tools to accelerate the embedded design process (see Figure 1). Together with selected partners, Altera offers a range of software development tools, hardware development tools, and development kits that include everything you need to quickly and easily create and implement a design.

- Software Development Tools
- Embedded Software Partners
- Hardware Development Tools
- Development Kits

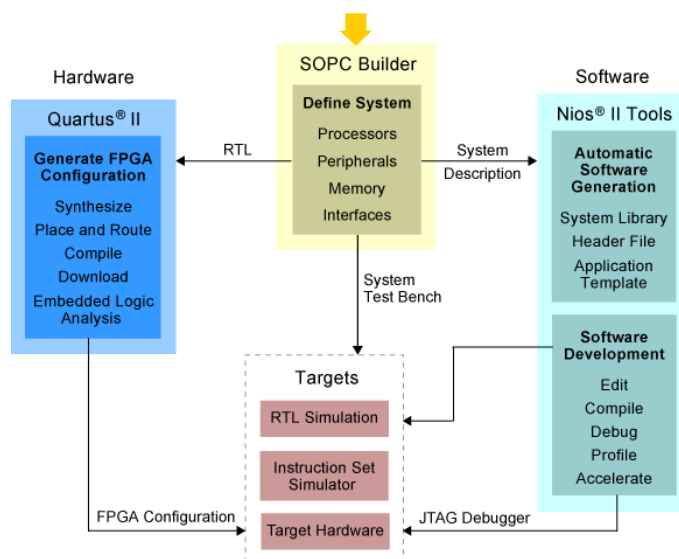
Software Development Tools

Altera, along with its embedded software partners, offers a range of powerful tools for your software development needs.

Nios II Embedded Design Suite

The Nios® II Embedded Design Suite (EDS) is a collection of components and tools used to develop embedded software for the Nios II processor, including Nios II Software Build Tools

for Eclipse based on the familiar Eclipse development environment. The Nios II IDE is also included to provide support for legacy designs. See what's new in the latest release.



Embedded Software Partners

Altera is proud to showcase several embedded software partners who provide the following products that support the Nios II processor.

- Operating systems
- Middleware

- Compilers
- Integrated Design Environments (IDEs)
- Debuggers
- Co-verification tools

Hardware Development Tools

Altera offers a range of hardware development tools that enable the highest levels of

productivity and the fastest path to design completion for high-density FPGA designs.

Quartus II FPGA System Design Tool

Altera's Quartus® II software leads the industry as the most comprehensive environment available for FPGA designs, providing

unmatched performance delivery, efficiency, and ease-of-use.

SOPC Builder System-Level Integration Tool

SOPC Builder eliminates manual system integration tasks and allows you to focus on custom user logic design to differentiate your

system. All versions of the Altera® Quartus II design software include the SOPC Builder system generation tool.

SignalTap II Embedded Logic Analyzer

The SignalTap™ II logic analyzer is a system-level debugging tool that captures and displays real-time signal behavior in a “system

on a programmable chip” (SOPC), allowing you to observe interactions between hardware and software in system designs.

MegaCore IP Library

You can choose from Altera's comprehensive MegaCore® intellectual property (IP) library of peripheral functions such as IDEs, UARTs, interrupt controllers, and PCI bus bridges to build a custom function optimized for specific applications.

Altera's rapidly growing portfolio of standard bus interfaces allows you to add chip-to-chip,

board-to-board, or box-to-box connectivity to SOPC designs. The microsystems portfolio also includes megafunctions to seamlessly add external memory, Ethernet interfaces, PCI™, PCIe®, USB, and next-generation processor interfaces.

Embedded Systems Board Solutions

Altera Embedded System Development Kit, Cyclone III Edition



ALTERA Altera Corporation

The Altera Embedded Systems Development Kit, Cyclone III Edition is a complete development platform for prototyping embedded systems on Altera's low-cost, low-power FPGA family. This kit is an ideal choice for developers running Linux on the Nios® II processor. Download the Nios II Hardware Reference Design for Linux, Cyclone III (EP3C120) Edition Release R15 to give your design a head start.

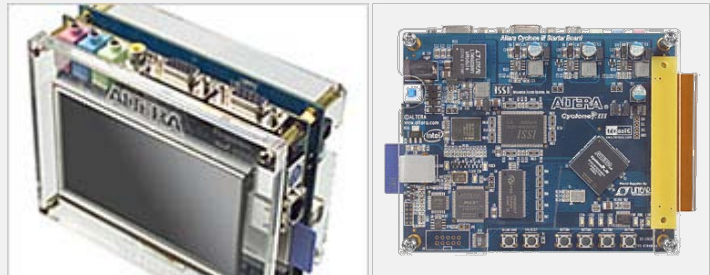
Features

- Altera Cyclone III EP3C120F780
- Development Hardware

- A Cyclone III FPGA-based board with high-speed mezzanine card (HSMC) connectors to interface to a wide range of daughtercards
- LCD multimedia HSMC to interface to common peripherals such as standard definition (SD) card, LCD color touch panel, etc. Multipurpose HSMC for software debugging and developing interfaces for USB 2.0 and Santa Cruz daughter cards
- The reference design includes:
 - Quartus II project file compatible with Quartus II software version 9.0 and later
 - Cyclone III FPGA development board design files

- U-boot files
- Out-Of-Box Experience
- This board is, in itself, an embedded system. On power-up, you can load a menu of "ready-to-run" demo applications. When connected to a network port, the Board Update Portal web page is served. From there, you can remotely update the board with a new design. See the user guide for details.
- This design is provided as a prebuilt processor system called the Nios II EP3C120 microprocessor system with LCD controller.

Nios II Embedded Evaluation Kit (NEEK), Cyclone III Edition



ALTERA Altera Corporation

The Nios® II Embedded Evaluation Kit, Cyclone® III Edition makes evaluating Altera's embedded solutions easier than ever. You can evaluate a dozen different processor systems targeting the low-cost, low-power Cyclone III FPGA by simply using the LCD color touch panel to scroll through and load your demo of choice. These processor systems showcase the unique benefits of FPGA-based processors such as reducing bill of material (BOM) costs by integrating powerful graphics engines within the FPGA, reducing operating costs by upgrading your system over the Internet, or increasing system performance while reducing power using the C-to-Hardware (C2H) acceleration compiler.

The Nios II Embedded Evaluation kit, Cyclone III Edition comes with a comprehensive suite for software development—the Nios II Embedded Design Suite (EDS)—as well as sample Nios II processor systems that include full source code.

Features

- Cyclone III Starter Board
 - Cyclone III EP3C25F324 FPGA
 - 32 MB of DDR SDRAM 1 MB of synchronous SRAM
 - 16 MB of Intel P30/P33 flash
 - Clocking : 50-MHz, on-board oscillator
 - Six push buttons total, four user controlled
 - Seven LEDs total, four user controlled

- LCD daughter card
 - Color LCD touch-screen display (800 x 480)
 - 24-bit CD-quality audio CODEC with line-in, line-out, and microphone-in jacks
 - 10/100 Ethernet physical layer/media access control (PHY/MAC)
- Connectors
 - VGA output
 - Composite TV-in
 - Audio-out, audio-in, and microphone-in
 - SD card
 - Serial connector (RS-232 DB9 port)
 - PS/2
 - Ethernet connector (RJ-45)
- Nios II Evaluation Kit CD-ROM

MAX II Development Kit



ALTERA Altera Corporation

The MAX II Development Kit enables you to evaluate the MAX II CPLD feature set or begin prototyping your own design. It includes reference designs (LCD controller, PCI, USB, and slot machine), demo designs, software, cables, and all the accessories needed to ensure fast and easy use of the MAX II CPLD.

Features

- Altera
 - MAX II CPLD EPM1270F256C5ES
- Active I/O sense circuit—Allows users to load VCCINT and observe the effect on MAX II user I/O ramp times

- Power measuring circuit—Allows users to measure the stand-by and nominal power consumed by the MAX II device
- Schmitt trigger circuit—Allows users to generate a custom clock using the internal Schmitt trigger
- 66-MHz oscillator
- Temperature sensor
- Four user-definable push-button switches
- Four user-definable LEDs
- 16 x 2 character LCD
- SRAM
- USB Interface V1.1 or V2.0
 - Type B connector
- 32-bit PCI edge connector

- Altera expansion prototype header
- Prototyping area

MAX V Starter Kit



gfec Galaxy Far East Corp.

Galaxy's "MAX V Starter Kit" is a simulation board specially made for the Altera MAX V Family of Devices. Those interested in digitizing design could realize their ideas through this experimental board. The built-in CPLD: 5M1270ZT144C5N provides 1270 LEs with 114 common I/O, 8K bits User Flash Memory. Detailed information and specifications are available on the DVD enclosed or on the Altera Web Site (<http://www.altera.com>). Except IC: 5M1270ZT144C5N, some peripheral parts connected to it, are available for users upon completion of a digital logic design.

Features

- Altera
 - MAX V CPLD EP5M1270ZT144C5N

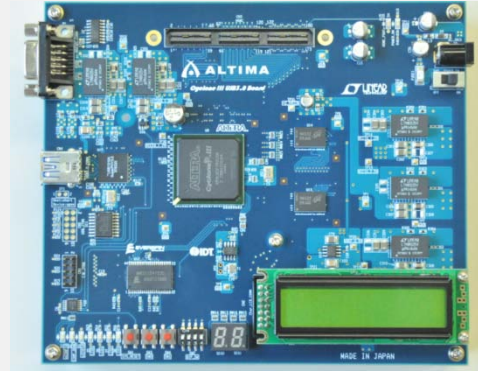
- Peripheral parts
 - 4 Bits DIP Switch
 - 2 Push Buttons
 - 8 LEDs
 - 1 Oscillator Socket
 - 4 Extension I/O Connectors
- EP5M1270ZT144C5N provides 114 common I/O pins. The expansion I/O ports of this experimental board connect to JP6 (IO 1), JP5 (IO 2), JP4 (IO 3) and JP7 (IO 4), respectively, so that the user can easily link this connector to other PC boards. Furthermore, JP6, JP5 and JP7 also provide the Power Pin and GND pin; Power Pins offer 1.2V, 1.5V, 2.5V and 3.3V voltages but without current protection.

- The voltage regulator has been built-in to this experimental board; power can be obtained by inserting a USB cable into USB connector.

Deliverables

- Altera MAX V Main Board
- USB Cable
- CD-ROM

Cyclone III USB3.0 Board



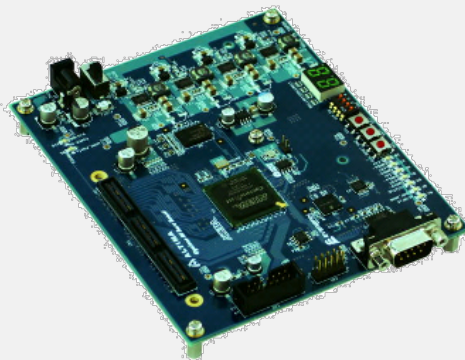
ALTIMA Corp.

Altima's "Cyclone III USB 3.0 Board" is an evaluation board for USB 3.0 interface by combining FPGA and USB 3.0 PHY devices. The user of this board can attain higher flexibility in setting up different evaluation configurations in USB 3.0 controller functions implemented in Cyclone III low cost FPGA. Also, the user can utilize HSMC connector to bridge to various interface standards at the same time.

Features

- Altera
 - Cyclone III FPGA EP3C80F780C6
 - Configuration ROM EPCS64
- Texas Instruments (TI) · TSUB1310 USB 3.0 PHY
 - Can be configured for both host cost and function controllers
- External IO
 - Altera's standard connector HSMC (High Speed Mezzanine Connector)
- CPU
 - ALTRA Nios II (32-bit RISC)
- Memory
 - Flash 16M Bytes
 - DDR2-400 128M Bytes x2
 - MRAM Everspin MR2A16AYS35 512KByte
- I/O Interface
 - USB 3.0 Standard-A Connector
 - RS232C
- User I/F
 - Push SW
 - DIP SW
 - LED
 - 7-Seg
 - Char LCD
- AC Adapter (12V DC-IN)

Cyclone III Base Board (Aquamarine)

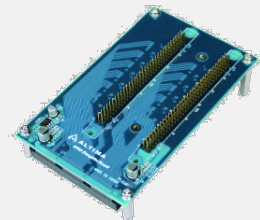


ALTIMA Corp.

Altima's Cyclone III Base Board is a platform for the customers designing with FPGA for the first time. The peripheral user interface such as 7-Seg, LEDs, and various switches provides highly visible environment for design circuitry. Also, the on board HSMC connector provides flexibility in expanding various I/O interfaces by connecting daughter boards such as the option GPIO and EPSD boards from Altima.

Features

- Altera
 - Cyclone III FPGA EP3C16F484C8, EP3C40F484C8N or EP3C55F484C8N
 - EPCS4 configuration ROM
- Everspin MRAM (Magnetoresistive RAM) 4Mb (512K x8 bit) MR2A08AM35 as instruction program memory for Nios II processor
- DDR2-333 128MB
- FLASH ROM (16M byte) MR2A08AM35
- IDT Versa Clock
- 3.3V interface GPIO HSMC daughter board (option)
- Serial connector (RS232 DB9)
- 7-Seg display x 2
- LED
- DIP Switch
- Push Switch
- Character LCD interface connector (character LCD is provided separately)
- HSMC expand IO connector



GPIO Daughter Board

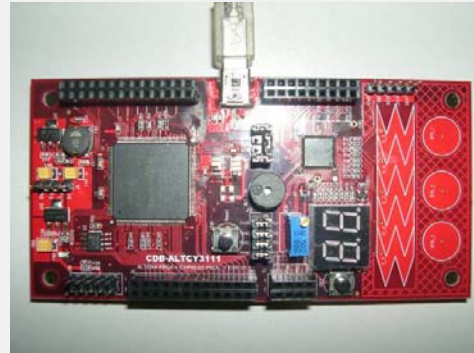
ALTIMA Corp.

GPIO Daughter Board (option) connects with Cyclone III Base Board from ALTIMA Corp. through HSMC connector. While HSMC's interface is specified to be at 2.5V, the IOs from HSMC can be used at 3.3V by using this board.

Features

- External IO: Altera HSMC Connector
- Voltage Level Transistor: TXB0108 (8 bit bidirectional type)
 - 2.5V HSMC ↔ 3.3V GPIO
- 88 pin User IO

Altera FPGA + Cypress PSoC EVK



Cytech Technology, Ltd.

Cytech's "Altera FPGA + Cypress PSoC EVK" is a starter kit for Altera Cyclone III FPGA and Cypress PSoC1. The kit provides a set of low cost, easy and convenient tool for learning FPGA and PSoC and for R&D using FPGA and PSoC.

Features

- Altera
 - Cyclone III FPGA EP3C5E144C8
 - Configuration ROM EPCS4S18
- Cypress
 - CY8C24894-24LFXI
 - CY7C1041DV33-10ZSXI
 - CY25701

- PSoC + FPGA + SRAM integrated
- CapSense
 - Three CapSense Buttons
 - One CapSense Slider
- User Interfaces
 - Two 7-Segment LEDs
 - Buzzer
 - 2 Switches
- ADC simulation on board
- External Interface
 - I2C / SPI
 - JTAG
 - USB
 - UART

- GPIOs pulled out
- Documentation and support deliverables
 - Schematics
 - PCB data
 - BOM list
 - User guide Firmware sample source code

Galaxy NIOS Starter Kit



Galaxy Far East Corp.

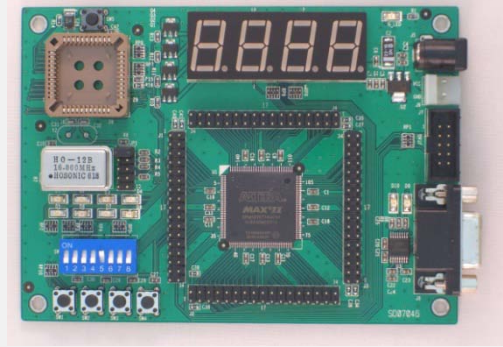
Beside FPGA device, Altera provide IP & development system for FPGA design, the Nios II is a 32 bit embedded processor, through Altera's SOPC (System on programmable Chip) Builder software, designer is very easy to integration Altera's IP such as embedded processor, DDR/DDRII SDRAM memory interface, UART, LCD module, timer and so on. Just pickup IP of SOPC Builder and few setting, the integration IP process is completed. The SOPC Build is connecting all IP interfaces, locating address range, assigning interrupt number, generating control logic and basic simulation model, OS and software driver automatically. Completing a system level hardware design need 10 minutes time only.

Features

- Altera
 - Cyclone II FPGA EP2C20F484C8
- 16M Bytes SDRAM Memory (MT48LC4M32B2)
- 8 M Bytes Flash Memory (AM29LV065D)
- 2X16 Character LCD Module
- PS2 Keyboard Interface
- RS232 Serial Communication Port
- 4 Bits DIP Switch
- 5 Push Button Switches
- 8 LEDs
- 50 Mhz Oscillator
- Provide 185 In/Out Pin & 128 shareable In/Out Pin

- Galaxy USB Blaster
- USB Cable
- Module Board Size : 111mmX90mm
- Extender Board Size: 221mmX172mm
- Board size: 130mm x 90mm

Galaxy MAX II Starter Kit



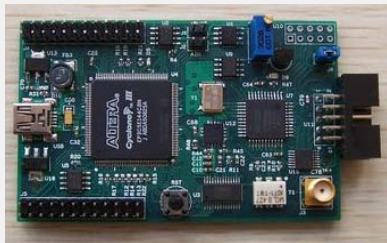
Galaxy Far East Corp.

The MAXII Starter kit provide a tool of enter FPGA/CPLD world , Anybody can use Altera free web edition software Quartus II study FPGA/CPLD design technique more easier. The Altera's MAXII family is a high volume low cost product, it provide bigger logic capacity and lower power consumption than tradition CPLD.

Features

- Altera
 - MAX II CPLD EPM1270T144C5
- 4 Digitals seven segment LED Display
- 8 Bits DIP Switch
- 4 Push Button Switchs
- 8 LEDs
- 1 x 16Mhz Oscillator
- 1 UART Connector
- 4 Extension I/O Connectors 114 I/O Pin
- 44 Pin Socket (for 3.3V 8051 CPU)
- JTAG Port Connector

Board Solutions from Third Party Board Partners



Mini FPGA Dev Kit

Hangzhou Free Electron Co. Ltd

It's a mini dev kit for engineers who want to study FPGA. This kit is small and the price is very low. Two daughter card are optional for customer if they want to develop Ethernet or Audio application.

Features

- FPGA device:EP3C5Q208C8N (upgradeable to EP3C10)
- Configuration device: EPCS4
- RAM:512K SRAM
- DAC: 10bit, 1.25M DAC, 14bit, 165M DAC(optional)
- ADC: 10bit, 1.25M DAC
- One LED, one SW push button, 24MHz Oscillator
- Two 24 pin expand port, each can expand 20 IO and 4 Clock
- Two daughter cards are optional for customers
- Very cheap price



Network daughter card

Hangzhou Free Electron Co. Ltd

This card is an option daughter card for Mini FPGA Dev Kit.

Features

- RJ45 connector
- 10/100 Ethernet MAC/PHY
- Connects with Mini FPGA Dev Kit with 2 x 24 pin expand port connectors



EDA-004 - Altera Cyclone III USB-FPGA board

Humandata Ltd.

Features

- Cyclone III FPGA EP3C55F780C8N (55K LE)
- Config. ROM: EPCS16SI8N or EPCS16SI16N
- Resister-protected 100 I/O pad 2.54 mm grid
- FPGA configuration through JTAG
- FPGA configuration through USB
- User communication through USB (FT2232H Sync-FIFO mode is available)
- 50 MHz Oscillator (50 ppm) or External input
- One User Push-Button Switch
- Tree User LEDs
- Two Status LEDs (Power, Done)
- MRAM (EVERSPIN, MR2A16AYS35 256Kx16)
- Power-on Reset signal for FPGA configuration
- JTAG port (10 pin socket) for ByteBlaster [MV/III] or USB Blaster
- Credit-Card-Size 3.386" x 2.126" (86 x 54 mm)



ACM-022 - Altera Cyclone III F780 FPGA board

Humandata Ltd.

Features

- ALTERA Cyclone III FPGA EP3C55F780C8N (55K LE) or EP3C80F780C8N (80K LE) or EP3C120F780C8N (20K LE)
- Configuration Device Altera EPCS64SI16N
- 100 I/O PAD 2.54 mm grid
- Separable VCCIO
- 30 MHz/50 MHz Oscillator (50 ppm) or External
- One User Push-Button Switch
- One User LED
- Two Status LEDs (Power, Done)
- SDRAM (Micron MT48LC16M16)
- MRAM (EVERSPIN MR2A16AYS35 256Kx16)
- Power-on Reset
- JTAG port (10 pin socket) for ByteBlaster[MV/II] or USB Blaster
- Credit-Card-Size 3.386" x 2.126" (86 x 54 mm)



ACM-202 - Altera Cyclone III F780 FPGA board

Humandata Ltd.

Features

- ALTERA Cyclone III FPGA EP3C55F780C8N (55K LE) or EP3C80F780C8N (80K LE) or EP3C120F780C8N (120K LE)
- Configuration Device Altera EPCS64SI16N
- 100 I/O PAD 2.54 mm grid
- Separable VCCIO
- 30 MHz/50 MHz Oscillator (50 ppm) or External
- One User Push-Button Switch
- One User LED
- Two Status LEDs (Power, Done)
- SDRAM (Micron MT48LC16M16)
- MRAM (EVERSPIN MR2A16AYS35 256Kx16)
- Power-on Reset
- JTAG port (10 pin socket) for ByteBlaster [MV/II] or USB Blaster
- Credit-Card-Size 3.386" x 2.126" (86 x 54 mm)



Altera DE2-115 Development and Education Board

Terasic Technologies

Features

- Cyclone IV EP4CE115 with ~114,480 LEs
- 2 Gigabit Ethernet Ports, HSMC connector
- 128MB SDRAM, 2MB SRAM, 8MB Flash
- User interfaces: 18 switches and 4 push-buttons, 18 red and 9 green LEDs, Eight 7-segment displays and 16x2 LCD module
- 24-bit encoder/decoder (CODEC) with line-in, line-out, and microphone-in jacks
- SD Card Socket
- USB Type A and B (host and device controller compliant with USB 2.0)
- 40-pin Expansion Port
- VGA-out Connector
- DB-9 Serial Connector
- PS/2 Connector
- Remote Control Infrared receiver module
- TV-in Connector (TV decoder NTSC/PAL/SECAM)

ASIC Prototyping

Why use FPGAs for ASIC prototyping?

In the modern ASIC design flow, the use of logic simulator software had been a relevant choice of technique for ASIC designers for long time as the older process ASIC had limited size of the designs. Also, the lower cost of the mask iterations allowed the designers to spin the design several times per project.

The traditional design and verification flow is a sequential flow as follows:

- (1) Verify the ASIC design using logic simulator and static timing analyzer tools
- (2) Develop the evaluation board and ASIC engineering sample (ES)
- (3) Verify both hardware and software (system verification) using the outcome of (2)
- (4) Redesign and build (2) if any bugs are found because the mask cost was reasonable

The mask cost for the latest ASIC process exceeds multiple million dollars recently, and it is almost prohibitive to reiterate the ASIC design while the product life cycle is shortening and the workload for software verification is widening.

The following illustration explains how the introduction of prototyping by FPGA dramatically changes the ASIC development flow.

Advantages of FPGA prototyping

The verification of design using FPGA can be done at faster speed in operation and in parallel by which shorter time of total verification can be attained. It is also effective for reducing the risk of ASIC chip design reiteration by specification change.

Faster operation speed of verification

The prototype design in FPGA can operate in the speed of as fast as hundreds of MHz. Even the very expensive emulator costing more than a few million dollars and the high level verification tools using C language can attain only a few MHz at the fastest. The verification speed using FPGA prototype is predominantly higher and closer to the speed of the final product.

Moreover, because the test pattern is input directly from the system, the verification engineers can skip the process of generating detailed test bench and expectation values but the result is observed in the actual system. This will result in reduction of workload to check and match the actual output and the expected results in great deal.

The recommended verification flow in general is:

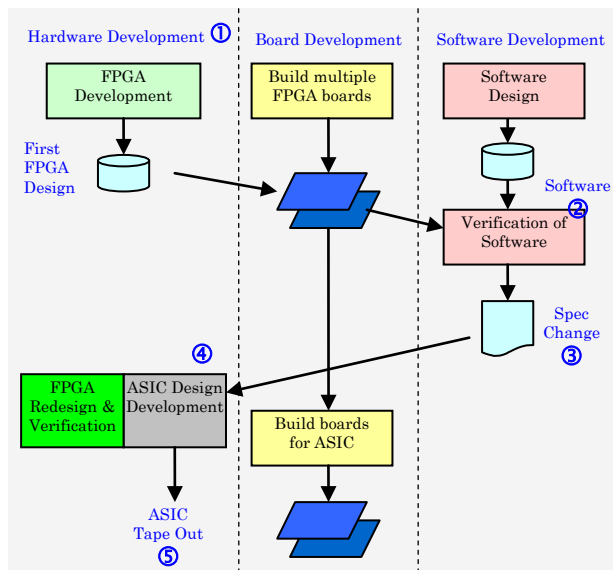
- (1) Design the system architecture by C language and verify
- (2) Verify the logic between function blocks using logic simulator
- (3) Build the FPGA prototype and verify the system

For instance, it is very difficult to use waveform for evaluating the picture images by different algorithms. The verification using the FPGA prototype enables the engineers actually see the output images against various image source data.

Parallel verification

The FPGA prototyping method allows the hardware design and software verification simultaneously (hardware-software co-design). The verification period can be dramatically reduced by verifying software by functionality on multiple prototype boards in parallel.

The figure shows how the parallel verification improves the verification process in the design flow.



① First Level FPGA Design

The FPGA designers first design the internal block of FPGA to communicate with software and external devices so that the software and board hardware design verification can be started even before the completion of the FPGA design. The FPGA designers pass out the FPGA functional block design to software engineers after verifying basic functionality by logic simulation.

② Software Verification

Software designers verify the software using the FPGA board and FPGA design passed to them as the result of the process 1. It is

common that the verification is done in multiple boards by functionality or by the engineer in parallel. (Parallel software verification: Parallel board – software verification)

During this process the FPGA designers continue the work on the design to add other functional blocks needed and improve the design quality of the total FPGA design. As the design of the FPGA is improved, it is passed each time to software engineers for verification. (Parallel logic design – software verification)

③ Specification Change

As the verification of the system continues, there can be the need to revise the partitioning between hardware and software processes, changes in other devices on the board, I/O specification changes on the FPGA, etc. As needed, project managers discuss the changes in specification and work on the changes to improve the system operation. Going through this process, the risk of revisions in the ASIC design by specification changes can be minimized. (Parallel specification making – system verification)

④ ASIC Design Development

As the design quality of the FPGA design continues to improve, the ASIC design development is started in parallel with the system verification using the FPGA prototype. The verification using the FPGA prototype will be continued until the availability of ASIC engineering sample (ES) as small corner bugs can be found. (Parallel ASIC design – system verification)

Frequently Asked Questions

Following is the list of questions and answers for ASIC designers without experience of using FPGA.

Q1. Do we have to build the FPGA board on our own?

A1. There are off the shelf ASIC prototyping board using FPGAs from various vendors. Please consult with your local Altera distributors (Altima, Elsen, Cytech, Galaxy) for details.

If these boards satisfy your specifications and functions (FPGA density per board, architecture for scaling the density, I/O types and speed, memory requirements, etc), it is highly recommended to use those to reduce the time and efforts to design, build and verify the board. If not, you are encouraged to build your own board.

Q2. How do you do the debugging on the FPGA?

A2. Unlike in ASICs, you can check the internal operation of the FPGA while it is in operation. You will not need oscilloscope or logic analyzer but you can observe the waveform of internal signals in operation by just preparing the FPGA design environment. However, the debugging with FPGA in operation is not easier compared with the use of logic simulator. It is recommended to use logic simulator for basic and main functionalities first, and move to FPGA system verification for smaller bugs.

Q3. As the high level design methodology like C language becomes common, will the FPGA prototyping be obsolete?

A3. The high level design methodology like C language is effective for applications with frequent update of algorithms as it requires less man power than RTL design. However,

the simulation speed is usually very slow as several MHz and the total time needed for FPGA prototyping is much faster.

It is more realistic to use the high level verification for algorithm and FPGA prototyping for system verification. It is also said that while C language is more sophisticated for algorithm development, the experiment on the physical level is very much important to utilize the human intellectual activities in the brain.

This is the reason why the FPGA prototyping method is widely utilized at laboratories for concept building and proof of concept works.

High level design:

Verify the idea in mind by simulator (no more evolving of the idea)

FPGA prototyping:

New idea can be found from the results different from initial expectation

Q4. Do you have to design ASIC and FPGA differently?

A4. In the case the ASIC design is too big to fit in one FPGA, you have to partition the design. Also in the case the performance of FPGA does not meet requirements, the design need to be changed to fit the architecture of the FPGA. Normally the same RTL design can be shared between ASIC and FPGA.

In the logic emulator you can use the ASIC design as is, but in reality the emulators use multiple FPGAs for the hardware part. The emulators tend to operate at lower performance than FPGA prototype as emulators are coupled with gimmicks to automatically partitioning the design and improve the ease of debugging.

Q5. Can you do the timing verification?

A5. Unfortunately, you cannot do the timing verification on the FPGA prototype as the timing for ASIC and FPGA are different. However, doing the functional verification on the FPGA board is a very effective way to reduce reiteration of ASIC designs as the most common reason for ASIC re-spin is the functional errors.

Altera FPGAs use the same Synopsys Design Constraints (SDC) used in ASIC design for FPGA timing constraints. So, the transition of timing constraint information is smoothly done between FPGA and ASIC.

Q6. What are the drawbacks in FPGA prototyping?

A6. Those relying too much on FPGA prototyping sometimes start skipping the

process of specification writing and logic simulation.

Without specification sheet the development can be delayed by going back and forth between physical verification and small specification changes again and again, or it may take more time to debug on the board by skipping logic simulation. However, these are not the disadvantage of FPGA prototyping but it is more of a lack of design flow or project management.

The FPGA prototyping method is effective in reducing the total time for development by operating the verification and design in parallel, but it requires more human resources. In the case you choose to employ the FPGA prototyping, our recommendation is to consult with design houses with FPGA design experience.

ASIC Prototyping Board Solutions

Stratix IV ASIC Prototyping Board EK4SEH40



GFEC Galaxy Far East Corp.

Altera Stratix IV-E FBGA1517 FPGA Prototyping Module

The module use Altera Stratix IV-E family FPGA with FBGA (Fine Line Ball Array) 1517 pin package device . Each extended I/O signal through protection buffer, provide 5V tolerance feature.

Features

- Altera Stratix IV Family FineLine BGA 1517 pin Package Device(EP4SE530 to P4SE820) up to 813,050 LEs, 23,130K RAM Bits, 960 18X18 Multipliers & 12 PLLs
- Altera Serial Configuration Device EPCS128
- 2 UART Serial Communication Port

- Oscillator Socket
- Provide 757 In/Out Pin (With I/O Protection buffer)
- 1 Mictor Connector
- Power System For Altera device (1.1V/3.0V/2.5V)
- 8 Separate I/O Bank
- Heat Sink Fan
- JTAG Port Connector
- AS Port Connector
- Battery for Stratix IV Security System
- Accessories
 - AC-Adapter x 1 piece (Power Adaptor of AC 110V/220V to DC 12V/5A)
 - GFEC USB Download Cable x 1

Altera Stratix IV-E FBGA1517 FPGA Prototyping Module

The module use Altera Stratix IV-E family FPGA with FBGA (Fine Line Ball Array) 1517 pin package device . Each extended I/O signal through protection buffer, provide 5V tolerance feature.

Features

- Altera Stratix IV Family FineLine BGA 1517 pin Package Device(EP4SE530 to P4SE820) up to 813,050 LEs, 23,130K RAM Bits, 960 18X18 Multipliers & 12 PLLs
- Altera Serial Configuration Device EPCS128
 - 2 UART Serial Communication Port

Board Solutions from Third Party Board Partners



ALL-IN-ONE Base Board B-11 (Stratix III Edition)

ACCVERINOS Accverinos Co.,Ltd.

Features

- EP3SL340F1517 or EP3SL200F1517 (-2 or -3)
- DDR2 DIMM
- DVI I/O Support: 1 each of input and output port using TI TFP403 & 410 chips. Max 165MHz
- 1 x Gigabit Ethernet PHY & RJ45 Connector.
- 1 x USB2.0 Connector, Cypress EZ-USB and ULPI supporting PHY - Can use either of USB MCU or PHY
- 8 pairs each of input and output signals through C44LVDS connectors. Tested 1.2Gbps/pair operation
- SD Card support (connected directly to FPGA and controlled by MegaCore IP)
- 1 x Altera standard HSMC connector
- 5 x Samtec 120-pin connectors

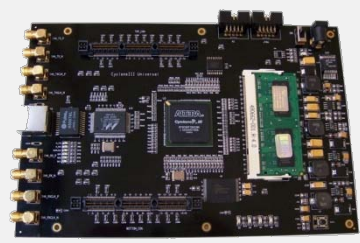


StarFire-2D820/530/340

Beijing HyperSilicon Co., LTD

Features

- Two Altera Stratix IV (EP4SE820 / EP4SE530 / EP3SL340F1760) FPGAs with capacity of 13.6 Million ASIC gates
- 760 connections between two FPGAs, with support for the AXI / APB / AHB bus standards.
- Stackable for two or more StarFire-2D820/530/340
- Optional SODIMM memory expansion slot, covering SDRAM, DDR, Mobile DDR, DDRII memory, with clock frequency up to 400MHz.
- 480 user I/Os
- 4 crystal sockets to provide clock input
- 4 SMA coaxial high speed I/Os
- A number of high-end power modules guarantee the power for the entire mother board and the extension of daughter boards as well



Cyclone III SOPC board

Hangzhou Free Electron Co. Ltd

This board offer Ethernet, DDR2 interface, enough test port and expend IO. It is suitable for SOPC system design and small/middle density IP/ASIC verification.

Features

- Cyclone III EP3C80F780C8N or EP3C120F780C8N
- 256M DDR2 SO-DIMM (up to 2G)
- 12 layer PCB
- 216 expand IO/CLK/PLL OUT (include 9 LVDS in, LVDS out)
- Marvel 10M/100M/1000M Ethernet PHY
- SMA clock/data input/output
- 32M FLASH
- 4 x LED, one reset



S4 TAI Logic Module for SOC prototype



S2C Inc.

This platform used 2 pcs Altera StratixIV (EP4SE530 /EP4SE820) FPGA, can verify 16.4M ASIC gate design.

Features

- Up to 66Mbits of FPGA internal memory
- Up to 2720 embedded 18x8 Multipliers
- One on-board DDR2 SO-DIMM socket
- One on-board DDR3 SO-DIMM socket
- Stackable to meet even larger gate count needs
- Up to 416 dedicated IO per FPGA
- Up to 454 shared nets and IOs for dual FPGA
- 20 user clocks from
 - 2 oscillator sockets
 - 3 pairs of differential SMB clock inputs
 - 3 programmable clock source (1-195MHz)
 - 12 feedback clocks from any user FPGA
 - 20 clock sources from J1 connector



DE3 Development System



Terasic Technologies

Features

- Stratix III 3SL150, 260 or 340
- DDR2 SO-DIMM socket
- 4 push-button switches, 1 DIP switch (x8) and 4 slide switches
- 8 RGB LEDs
- 2 seven-segment displays
- USB Host/Slave Controller with one mini-AB for host/device and two type A for device
- SD Card socket
- 50MHz onboard oscillator for clock source
- 1 SMA connector for external clock input
- 1 SMA connector for PLL clock output
- Eight 180-pin High Speed Terasic Connectors (HSTC), where 4 male and 4 female connectors are on the top and bottom of DE3, respectively.
- Two 40-pin Expansion Headers

Contact Information

For product details and inquiries, please contact your local Macnica Group companies with Altera franchise.

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